



KTH Electrical Engineering

Modeling Analog to Digital Converters at Radio Frequency

Niclas Björzell

Doctoral Thesis in Telecommunications
Stockholm, Sweden 2007

TRITA-EE 2007:062
ISSN 1653-5146
ISBN 978-91-7178-777-4

KTH School of Electrical Engineering
SE-100 44 Stockholm
SWEDEN

Akademisk avhandling som med tillstånd av Kungliga Tekniska Högskolan framlägges till offentlig granskning för avläggande av teknologie doktorsexamen i telekommunikation fredagen den 30 november klockan 13.00 i sal 99:131 på Högskolan i Gävle, Kungsbäcksvägen 47, Gävle.

© Niclas Björsell, oktober 2007
Tryckt av Universitetsservice US AB

Abstract

This work considers behavior modeling of analog to digital converters with applications in the radio frequency range, including the field of telecommunication as well as test and measurement instrumentation, where the conversion from analog to digital signals often is a bottleneck in performance. The models are intended to post-process output data from the converter and thereby improve the performance of the digital signal. By building a model of practical converters and the way in which they deviate from ideal, imperfections can be corrected using post-correction methods.

Behavior modeling implies generation of a suitable stimulus, capturing the output data, and characterizing a model. The demands on the test setup are high for converters in the radio frequency range. The test-bed used in this thesis is composed of commercial state-of-the-art instruments and components designed for signal conditioning and signal capture. Further, in this thesis, different stimuli are evaluated, theoretically as well as experimentally.

There are a large number of available model structures for dynamic nonlinear systems. In order to achieve a parameter efficient model structure, a Volterra model was used as a starting-point, which can describe any weak nonlinear system with fading memory, such as analog to digital converters. However, it requires a large number of coefficients; for this reason the Volterra model was reduced to a model structure with fewer parameters, by comparing the symmetry properties of the Volterra kernels with the symmetries from other models. An alternative method is the Kautz-Volterra model, which has the same general properties as the Volterra model, but with fewer parameters. This thesis gives experimental results of the Kautz-Volterra model, which will be interesting to apply in a post-correction algorithm in the future.

To cover behavior not explained by the dynamic nonlinear model, a complementary piecewise linear model component is added. In this thesis, a closed form solution to the estimation problem for both these model components is given. By gradually correcting for each component the performance will improve step by step. In this thesis, the relation between a given component and the performance of the converter is given, as well as potential for improvement of an optimal post-correction.

Sammanfattning

Det här arbetet handlar om att ta fram beteendemodeller av analog till digital omvandlare avsedda för tillämpningar i radiofrekvensområdet. Det gäller tillämpningar inom telekommunikation men även in test- och mätinstrument där omvandlingen från analoga till digitala signaler ofta är en prestandamässig flaskhals. Modellerna är avsedda att användas för att efterbehandla utdata från omvandlaren och på så sätt förbättra prestanda på den digitala signalen. Genom att skapa modeller av verkliga omvandlare och hur dessa avviker från ett idealt beteende kan ofullständigheter korrigeras genom så kallad postkorrigering.

Beteendemodeller innebär att genererar en lämplig insignal, mäta utdata och beräkna en modell. För omvandlare i radiofrekvensområdet ställs höga krav på instrumentering. Den testutrustningen som används är baserad på moderna högprestanda instrument som har kompletterats med specialbyggd utrustning för signalkonditionering och datainsamling. I avhandlingen har även olika insignaler utvärderats med såväl teoretisk som experimentell analys.

Det finns ett flertal olika varianter av modeller för att modulera ett olinjär, dynamisk system. För att få en parametereffektiv modell har utgångspunkten varit att utgå från en Volterramodell som på ett optimalt sätt beskriver svagt olinjära dynamiska system, så som analog till digital omvandlare, men som är alltför omfattande i antal parametrar. Volterramodellens har sedan reducerats till en mindre parameterintensiv, modellerstruktur på så sätt att Volterrakärnans symmetriegenskaper jämförts med symmetrierna hos andra modeller. En alternativ metod är att använda en Kautz-Volterramodell. Den har samma generella egenskaper som Volterramodellen, men är inte lika parameterkrävande. I den här avhandlingen redovisas experimentella resultat av Kautz-Volterramodellen som i framtiden kommer att vara intressanta att använda för postkorrigeringen.

För att kunna beskriva beteenden som en dynamiska olinjära modellen inte klarar av har modellen kompletterats med en statisk styckvis linjär modellkomponent. I avhandlingen presenteras en sluten lösning för att identifiera samtliga paramervärden i modellen. Vidare har det i avhandlingen genomförs en analys av hur respektive komponent påverkar prestanda på utsignalen. Därigenom erhålls ett mått på den maximala prestandaförbättring som kan uppnås om felet kan elimineras.

Acknowledgments

I would like take the opportunity to extend my greatest gratitude to my supervisor Professor Peter Händel for his guidance and supervision, his patience with my incomplete drafts, for a pleasant company on several conference journeys, and for being a never-ceasing source of idée's about ADC research activities.

Professor Peter Händel is the scientific leader at the research group at KTH in which I have been honoured to participate. I also want to thank my colleague PhD students in the research group: First, Dr. Henrik Lundin for valuable discussions, for introducing me to the network of researchers in the field of ADCs and companionship on several travels around the world. This is also true for Dr. Tomas Andersson, who left the group somewhat earlier but contributed in a positive way to the progress in my work. Finally, Mr. Samer Medawar who recently started his journey towards sound knowledge about ADC characterization.

My thanks also to my assistant supervisor Professor Niclas Keskitalo, who introduced me to the research group at KTH, and for the way he is steering our research project at University of Gävle. Within the project, I would like to thank all of you who have helped and supported me in various ways. Especially, I want to thank two of my co-authors: Dr. Daniel Rönnow as a creative initiator to the papers he contributed in and Mr Olav Andersen who, beside from being a co-author, essentially contributed to the design of the test-bed and spent some long days in the laboratory sharing his great knowledge and experience. I would also like to thank Dr. Magnus Isaksson for collaboration leading to a joint publication, Mr. David Wisell and my other co-authors Dr. Magnus Jansson and Mr. Petr Suchánek.

The University of Gävle and Professor Edvard Nordlander has providing financial support. The work was also supported by Ericsson AB, Freescale Semiconductor Nordic AB, Infineon Technologies Nordic AB, Knowledge Foundation, NOTE AB, Racomma AB, Rohde&Schwarz AB and Syntronic AB.

I also sincerely want to thank all the people in the department ITB/Electronics at the University of Gävle as well as PhD students within GST (Graduate school of telecommunication) for their contribution towards creating a very stimulating working environment.

Lastly, I want to express my greatest gratitude to my family, especially my wife Ann-Marie and my two sons Joachim and Filip, whose understanding, encourage and patience have made this work possible.

*Niclas Björsell
Gävle, October 2007.*

TABLE OF CONTENTS

APPENDED PAPERS	IX
RELATED PAPERS NOT INCLUDED IN THE THESIS.....	X
1 INTRODUCTION.....	1
1.1 Background	1
1.2 Outline and Contribution of the Thesis.....	2
2 ADC TESTING AND CHARACTERIZATION	3
2.1 Frequency Domain Performance Measures.....	3
2.2 ADC Integral and Differential Nonlinearity	5
2.3 Test Set-up and Device under Test	7
2.4 Histogram Tests and Input Stimuli.....	8
2.5 Comparing Different Stimuli.....	12
3 MODELS.....	17
3.1 Dynamic Nonlinear Models	18
3.2 Measuring Volterra Kernels.....	20
3.3 Dynamic INL Modeling for ADC Characterization.....	21
3.4 A Closed Form Solution to the Estimation Problem.....	26
3.5 The Kautz-Volterra Model	28
4 MODEL-BASED POST-CORRECTION	31
4.1 Post-Correction Based on Parametric Models.....	31
4.2 Performance Analysis	32
5 DISCUSSION.....	37
SUMMARY OF APPENDED PAPERS	39

REFERENCES..... 43

Appended Papers

- PAPER I** N. Björzell and P. Händel, "Truncated Gaussian Noise in ADC Histogram Tests," *Measurement*, vol. 40, pp. 36-42, 2007.
- PAPER II** N. Björzell and P. Händel, "Histogram Tests for Wideband Applications," *IEEE transactions on Instrumentation and Measurement*, Accepted for publication, July 2007.
- PAPER III** N. Björzell, P. Suchánek, P. Händel, and D. Rönnow, "Measuring Volterra Kernels of Analog To Digital Converters Using a Stepped Three-Tone Scan," *IEEE transactions on Instrumentation and Measurement*, Accepted for publication, August 2007.
- PAPER IV** N. Björzell and P. Händel, "Achievable ADC Performance by Post-Correction Utilizing Dynamic Modeling of the Integral Nonlinearity," *EURASIP Journal on Advances in Signal Processing*, Submitted, April 2007, revision September 2007.
- PAPER V** N. Björzell, O. Andersen, and P. Händel, "High Dynamic Range Test-Bed for Characterization of Analogue-To-Digital Converters up to 500 MSPS," *14th IMEKO Symposium on New Technologies in Measurement and Instrumentation & 10th Workshop on ADC modelling and testing*, September 12-15, 2005, Gdynia, Poland , pp. 601-604.
- PAPER VI** P. Händel, N. Björzell, and M. Jansson, "Model Based Dynamic Characterization of Analog-Digital-Converters at Radio Frequency — Invited paper," in *2007 International Conference on Signal Processing and its Applications*, 12-15 February, 2007, Sharjah, UAE.
- PAPER VII** N. Björzell, M. Isaksson, P. Händel, and D. Rönnow, "Kautz-Volterra Modelling of an Analogue-to-Digital Converter Using a Stepped Three Tone Excitation," in *12th Workshop on ADC Modelling and Testing*, September 19-21, 2007, Iasi, Romania, pp. 107-112.

Related Papers not Included in the Thesis

- VIII** N. Björnsell and P. Händel, "Benefits with Truncated Gaussian Noise in ADC Histogram Tests," in *9:th Workshop on ADC Modelling and Testing*, September 29 - October 1, 2004, Athens, Greece, pp. 787-792.
- IX** N. Björnsell and P. Händel, "On Gaussian and Sine Wave Histogram Tests for Wideband Applications," in *IEEE Instrumentation and Measurement Technology Conference*, May 17-19, 2005, Ottawa, Ontario, Canada.
- X** N. Björnsell and P. Händel, "A Statistical Evaluation of ADC Histogram Tests with Arbitrary Stimuli Signal," in *5th International Conference on Advanced A/D and D/A Conversion Techniques and their Applications*, July 25-27, Limerick, Ireland, 2005, pp. 259-264.
- XI** N. Björnsell and P. Händel, "Analog-to-Digital Converters for High-Speed Applications," in *National Microwave Symposium GigaHertz 2005*, November 8-9, 2005, Uppsala, Sweden, pp. 148-151.
- XII** N. Björnsell, D. Rönnow, and P. Händel, "Measuring Volterra Kernels of Analog to Digital Converters Using a Stepped Three-Tone Scan," in *IEEE Instrumentation and Measurement Technology Conference*, April 24-27, 2006, Sorrento, Italy, pp. 1047-1050.
- XIII** N. Björnsell and P. Händel, "Dynamic Behavior Models of Analog to Digital Converters Aimed for Post-Correction in Wideband Applications" in *11th Workshop on ADC Modelling and Testing*, September 17-22, 2006, Rio de Janeiro, Brazil.
- XIV** N. Björnsell and P. Händel, "Post-Correction of Under-Sampled Analog to Digital Converters," in *IEEE Instrumentation and Measurement Technology Conference*, May 1-3, 2007, Warsaw, Poland.
- XV** S. Medawar, N. Björnsell, P. Händel, and M. Jansson, "Dynamic Characterization of Analog-Digital-Converters," in *Mosharaka International Conference on Wireless Communications and Mobile Computing*, 6-8 September, 2007, Amman, Jordan.
- XVI** P. Händel, N. Björnsell, M. Jansson and S. Medawar, "Modeling the Dynamics of Analog-Digital Converters at Radio Frequency," *The Conference on RF Measurement Technology, for State of The Art Production and Design*, September 11-12, 2007, Gävle, Sweden.

1 Introduction

1.1 Background

Today, most of the signal processing performed in electronic systems is digital, and the performance of the analog to digital converters (ADCs) present at the border of the digital domain become very important. The most recent applications in consumer electronics, telecommunication, and test and measurement instrumentation call for ever-increasing ADC resolution and speed. Price and power consumption are other determine properties of an ADC. The properties of the ADC depend on the architecture of the component; ADC architectures with very high resolution have low sampling rate and vice versa. The application will decide what ADC architecture will be most suitable to match the requested demands.

Five converter architectures are widely used to perform amplitude quantization: Flash, pipeline, integrating, successive approximation and sigma-delta. Each of these architectures has its own unique advantages and disadvantages, which should be investigated when determine which ADC best meets an application requirement (see e.g. [1])

Some applications require a combination of speed and resolution superior to what can be provided by the manufactured ADCs. A practical ADC can not fully provide the performance of an ideal, due to imperfections in the component. Thus, there is a potential for improvements if the effect from the imperfections can be minimized.

In ADCs, performance can be improved using dither. This is external noise which is added to the input to the ADC. The noise signal can be a narrowband signal outside the signal band of interest, subsequently subtracted after the ADC, or use a suitable filter at the output of the system can thus recover this small signal variation. Dithering will not be further considered in this thesis. The performance can also be improved by post-processing the ADC output data. Post-processing implies a characterization of the ADC behavior, and to use that information to calculate a correction factor that reflect any deviations from an ideal behavior. This method is generally referred to as post-correction.

Error modeling has played a main role in generating a correction of the ADC behavior. An online correction obtained by subtracting the modeled dynamic error to each output sample of the actual ADC. For an ideal ADC the output is a discrete time and discrete amplitude representation of the analog input signal with fixed time and amplitude steps. The output from a practical ADC has deviations from the ideal steps. Deviations in time steps are called jitter, and are not the topic of this thesis. An ADC-model contains information on the size of the amplitude deviation as a function of the output code, which can be used to correct the output, and, thus, give a better representation of the analog input. In methods using look-up tables (LUTs) [2-7] the post-correction information is stored in a table and the output code is addressing the information. The addition of one or more previous samples will improve the correction. However, such modeling approach has a main limitation; the error model

needs for its identification a burdensome experimental work. In model based post-correction, the post-correction term is computed from a mathematical model. A parametric model requires less memory size and does not need to be trained for every combination of present and previous samples. A well assigned model is able to describe scenarios for which it is not trained.

Modeling ADCs at radio frequency require a model structure suited to describe a nonlinear dynamic behavior. Moreover, the model has to be valid over a wide frequency range. The challenge is to find a model structure that is fairly easy to characterize with a minimum number of model parameters without any loss of information. In addition, the method for parameter estimation should be easy to use and the estimator should be efficient.

1.2 Outline and Contribution of the Thesis

This thesis can be divided into three major parts; ADC testing and characterization, ADC modeling, and model-based post-correction, where each part is described in a separate chapter.

Chapter 2 describes the test set-up [Paper V] and discusses and compares different stimuli for ADC characterization. In substance the contents is based on two papers, where both papers are using the histogram test as characterization method. In [Paper I], the Cramér-Rao lower bound and a minimum variance estimator for histogram tests with an arbitrary stimulus are derived. In [Paper II], a metrological comparison between two different stimuli, sine-waves and Gaussian noise is performed.

Chapter 3 starts with an introduction to different dynamic nonlinear ADC models. The main contents are three different dynamic nonlinear models obtained from measurements. First, describes how frequency domain Volterra kernels of an ADC are determined from measurements and that the Volterra kernels have the symmetry properties of a parallel Hammerstein box model [Paper III]. The parallel Hammerstein model is after that refined into a new model that includes a static, piecewise linear component in the model structure. In [Paper VI], a closed form solution to the estimation problem for that model is derived. Chapter 3 ends the third model structure, a Kautz – Volterra model [Paper VII].

The models described in Chapter 3 are aimed for post-correction. Chapter 4 describes some post-correction methods and the potential performance improvement when using model-based post-correction [Paper IV].

Finally, a summary of results are given in Chapter 5.

2 ADC Testing and Characterization

Testing ADCs is done to measure the parameters that define the ADC performance. Many algorithms and testing methods have been developed to characterize ADC behavior, to validate ADC models, and to allow for error corrections through software. Several test methods are described in the IEEE standard [8]; see also the review articles [9, 10].

The choice of critical ADC parameters and matching test methods is related to the application for which the ADC will be used. According to [9] most applications today can be classified into five broad market segments: 1) data acquisition, 2) precision industrial measurement, 3) voice band and audio, 4) high speed (with sampling rates greater than about 5 MS/s) and 5) control loop applications where ADCs are part of a feedback loop.

Analog to digital converters aimed for radio frequency are found in segment 4 (high-speed ADCs) where the application can be instrumentation, intermediate frequencies (IF) sampling, software radio or software driven measurements. The most commonly used ADC architecture for these applications is the pipelined ADCs.

Traditional static specification parameters for ADCs are often not sufficient to adequately characterize the device in these applications. Static errors are those that occur for slowly varying or constant signals. Dynamic errors are the additional errors that occur as the signal varies. For high-speed applications, it is important to measure both static and dynamic errors.

Testing ADCs demands high-performance instrumentation. The measurement system must be superior the ADC, so that the measured result represents the performance of the ADC without any interference from the test-bed. Moreover, finding and generating the appropriate test signals scenario is of importance. Some test scenarios require a digital pre-distortion so that the stimuli have the required spectral purity.

In this chapter, the most important specification for high-speed ADCs will be given. Section 2.1 essentially defines frequency domain parameters on a more general level, while parameters related to the linearity of the ADC are handled on detailed level in Section 2.2. The test-bed will be described in Section 2.3. Section 2.4 will give an overview of the histogram test and commonly used stimuli, and the chapter ends with a comparison between different stimuli in Section 2.5.

2.1 Frequency Domain Performance Measures

Commonly used measures of dynamic performance are often based on single-tone measurements; for example the *spurious free dynamic range (SFDR)*, *total harmonic distortion (THD)*, and the *signal to noise and distortion ratio (SINAD)*. In addition there are measures such as intermodulation products, *adjacent channel leakage ratio (ACLR)*, and missing tone that are characterized by multi-tone or wideband signals.

Hence, the choice parameter for evaluation is not obvious; it must be done in accordance with the application.

The *THD* is commonly used in the papers appended to this thesis to evaluate the ADC in the frequency domain. The *THD* is the ratio of the root-mean-square (RMS) value of the fundamental signal to the mean value of the root-sum-square (RSS) of its harmonics. The *THD* is a convenient figure of merit for non-linearity evaluations since non-linearity implies harmonic distortion in the output signal. Consequently, it will be a suitable parameter for evaluation of the extent to which we can use our knowledge of the non-linearity and thereby correct the signal to avoid harmonic distortion.

The measures used in this thesis are defined by the IEEE standard 1241 [8]. The definitions are given in the following subsections.

2.1.1 Total Harmonic Distortion (THD)

For a pure sine wave input of specified amplitude and frequency, the RSS of all the harmonic distortion components including their aliases in the spectral output of the ADC. Unless otherwise specified, *THD* is estimated by the RSS of the second through the tenth harmonics, inclusive. *THD* is often expressed as a decibel ratio with respect to the RMS amplitude of the output component at the input frequency.

2.1.2 Spurious-Free Dynamic Range (SFDR)

For a pure sine-wave input of specified amplitude and frequency, the ratio of the amplitude of the ADC's output averaged spectral component at the input frequency, to the amplitude of the largest harmonic or spurious spectral component observed over the full Nyquist band.

2.1.3 Signal-to-Noise and Distortion Ratio (SINAD)

For a pure sine wave input of specified amplitude and frequency, the ratio of the RMS amplitude of the ADC output signal to the RMS amplitude of the output noise, where noise is defined to include not only random errors but also nonlinear distortion and the effects of sampling time errors. One may notice that *SINAD* in IEEE standard 1241 [8] is equivalent to *signal-to-noise-ratio (SNR)* in IEEE Standard 1057-1994 [11].

2.1.4 Effective Number of Bits (ENOB)

A measure of the *SINAD* used to compare actual ADC performance to an ideal ADC. For an input sine wave of specified frequency and amplitude, after correction for gain and offset, the *ENOB* is the number of bits of an ideal ADC for which the RMS quantization error is equal to the RMS noise and distortion of the ADC under testing.

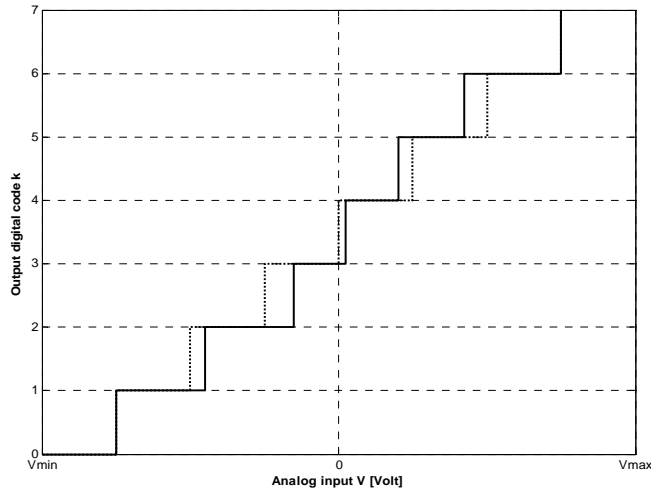


Figure 1: The relationship between the analog input signal v and the digital output code k from an ideal $B=3$ bits ADC (dashed line) and practical ADC (solid line).

2.1.5 ACLR Adjacent Channel Leakage Ratio (ACLR)

A figure of merit which is commonly used in telecommunication systems using WCDMA signals is $ACLR$, which is the ratio in dB between the measured power within a channel and the power in an adjacent channel.

2.2 ADC Integral and Differential Nonlinearity

The relationship between the analog input signal v and the digital output code k from an ideal ADC approximates the dotted staircase transfer curve shown in Figure 1. For the ideal ADC, the code transition levels T_k within the ADC range (V_{min} , V_{max}) are given by

$$T_k = Q(k - 1) + T_1, \quad (1)$$

where Q is the ideal width of a code bin; in other words, the full-scale range of the ADC is divided by the total number of codes $(V_{max} - V_{min})/2^B$, where B denotes the number of bits. Further, T_1 is the ideal voltage corresponding to first transition level, and T_1 is equal to $V_{min}+Q$ or $V_{min}+Q/2$ depending on the convention used: the 'mid-riser' convention or 'mid-tread', respectively [8]. The code k spans $k = 1, \dots, 2^B - 1$.

Due to imperfections in all practical ADCs, the transfer curve is often somewhat distorted, which is illustrated by the solid line in Figure 1. The actual code transition level $T[k]$ (that is, the ideal and practical transition levels are distinguished by the

placement of the argument k , viz. T_k and $T[k]$, respectively) is the voltage that results in a transition from ADC output code $k-1$ to k . *Integral nonlinearity (INL)* is described as the difference between the ideal T_k in (1) and the actual $T[k]$ code transition levels of the ADC after a correction has been made for gain and offset errors [8, 10]. Given the ideal code transition levels T_k in (1) and the measured levels $T[k]$, the correction is made by adjusting the gain G and offset V_{os} in order to 'minimize' the residual $\varepsilon[k]$ (for $k = 1, \dots, 2^B - 1$) [8]:

$$\varepsilon[k] = T_k - G \cdot T[k] - V_{OS} . \quad (2)$$

Equation (2) describes an over-determined set of $2^B - 1$ equations, with the two unknowns of interest G and V_{os} . According to the IEEE standard 1241 [8], different methods may be applied for determining the optimal (G, V_{os}) -pair such as the 'terminal based' method in which G and V_{os} are determined by the end-points only. This forces $\varepsilon[k]$ in (2) to zero for $k=1$ and $k = 2^B-1$, respectively. Another alternative is to minimize the sum of the squared errors in (2) with respect to G and V_{os} . The latter approach is denoted as 'independent based' gain and offset [8]. The *INL* as a percentage of the full scale range of the ADC is given by the normalized residual in (2), that is

$$INL[k] = \frac{100\% \cdot \varepsilon[k]}{2^B Q} . \quad (3)$$

The *INL* is normally expressed in least significant bits (LSBs), where a LSB is synonymous with one ideal code bin width Q ; that is $INL[k] = \varepsilon[k]/Q$.

Differential nonlinearity (DNL) is the difference, after correcting for the obtained static gain G , between a specified code bin width and the ideal code bin width Q , divided by the ideal code bin width. The *DNL* is given as follows

$$DNL[k] = \frac{W[k] - Q}{Q} , \quad (4)$$

where $W[k]$ is the corrected width of code bin k (that is, $W[k] = G(T[k+1] - T[k])$, with G determined by one of the two methods described above). One may note that, neither the width of the top bin $W[2^B-1]$ nor that of the bottom bin $W[0]$ is defined.

A code k is defined to be a missing code if [8]

$$DNL[k] \leq -0.9 . \quad (5)$$

Differential nonlinearity for an ideal ADC coincides with $DNL[k]=0$ for all $k = 1, \dots, 2^B - 2$, whereas the *INL* is zero for all $k = 1, \dots, 2^B - 1$. When *DNL* is given as one number without code bin specification, it is defined as the maximum

differential nonlinearity of the entire code range, or the maximum value of $|DNL[k]|$ for all k . In addition the RMS value of the DNL is commonly used and given by:

$$DNL_{RMS} = \left(\frac{1}{2^{B-1}} \sum_{k=1}^{2^{B-1}} DNL^2[k] \right)^{\frac{1}{2}}. \quad (6)$$

From (2), it directly follows that $\varepsilon[k+1]-\varepsilon[k]=Q-W[k]$, and thus the relation between $INL[k]$ and $DNL[k]$ is

$$DNL[k] = INL[k + 1] - INL[k]. \quad (7)$$

2.3 Test Set-up and Device under Test

The ADC test-bed is composed of commercial state-of-the-art instruments and components designed for this test-bed. An overview of the test set-up is shown in Figure 2. The clock signal is generated with a high quality signal generator. The clock signal can be adjusted via variable delays and filters to different requirements and applications. A vector signal generator (VSG) (R&S SMU200A) is the foundation input signals generation. Specially made, ultra low distortion and low noise IF amplifiers, as well as several custom-designed SAW filters and delay lines, are used for signal conditioning. A frame grabber (FG) acquires data from the ADC in real time. In addition to this equipment a second signal generator and a signal analyzer is part of the test set-up. The signal analyzer is used to examine and verify input signals. Moreover, the signal analyzer is also used to create a spectrally pure three tone signal (see Section 2.4.6). All instruments are connected to a computer via GPIB or local area network (LAN).

A high-performance signal generator is a key component for successful ADC characterization. Although it led to a larger investment, the signal generator can be used in various kinds of applications and is thereby standard equipment in most laboratories. The VSG combines up to two independent RF signal sources in one box, and it also offers unrivalled RF and base band characteristics including -160dBc/Hz phase noise at offsets >1MHz, I/Q modulator with 200 MHz RF bandwidth and frequency from 100 kHz to 3GHz. Arbitrary signals are generated in a PC-program (e.g. Matlab) and thereafter transferred to the VSG via a LAN.

Even with a state-of-the-art signal generator, additional signal conditioning is required. Filters are used to clean-up spurious noise from the test signal. However, the filters attenuate the signals; therefore, they have to be amplified to obtain the sufficient drive level (-0.5dBFS), which can be as high as +16dBm on some newer ADC's [12]. For that purpose, an ultra low distortion ADC driver has been designed with a frequency range of 20 - 300 MHz and 14dB gain. The amplifier ensures spectral purity even at high output levels by >80dBm output, a second-order intercept point (IP2) >49dBm IP3 and a noise level below -169dBm/Hz.

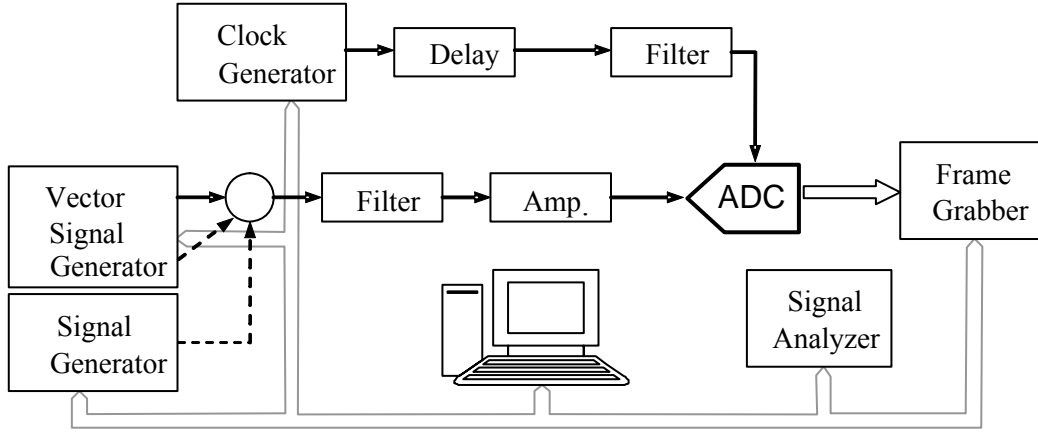


Figure 2: Schematic diagram of experimental set-up.

The FG acquires data from the ADC. A commercial state-of-the-art logic analyzer may be a solution, but using such an analyzer requires a large investment for a narrow field of applications. The logic analyzer solution has also been experiencing practical problems with false low level spuriousness from coupling of long parallel interconnection cables to the ADC under test. A design based on FPGA and high-speed memories is a cost-efficient alternative. The FG interface to the ADC under testing and in real-time record the binary represented samples at a maximum speed of 350 MHz (option for >500 MHz), width 16 bits, and depth 2 MSample (4 MByte). Samples are delivered from the ADC synchronously in binary format on low-voltage differential signaling (LVDS) busses. After the acquisition process is completed, the acquired data is uploaded to the PC over the LAN for analysis.

The device used for measurements and simulations throughout this thesis was a 12-bit pipeline ADC (AD9430) from Analog Devices. The maximum sampling rate is 210 MHz, and the analog bandwidth is 700 MHz. The simulation model is provided by the ADC manufacturer. All frequencies have been chosen according to coherent sampling.

2.4 Histogram Tests and Input Stimuli

The testing of ADCs with statistical analysis is based on building a histogram. The ADC histogram test method is considered to be an estimation problem in which the task is to estimate an arbitrary transition level $T[k]$ based on the ADC output. The histogram gives the number of occurrences of each code at the output of the converter for a given stimulus. This measured histogram (\hat{p}_k) is then used together with the probability density function (pdf) of the stimulus to estimate the actual code transition levels $T[k]$.

2.4.1 Different Stimuli Signals

An experimental problem when characterizing and modeling ADCs is that it is difficult to generate spectrally pure signals. This is particularly problematic when a model including a nonlinear memory effect is used. When identifying a nonlinear dynamic system, it is of course an advantage if a properly designed noise signal can be used, since it excites all frequencies (fundamentals, sums and difference frequencies) and all amplitudes. It is, however, difficult to generate distortion free noise signals. Thus, alternative stimuli can be used. The choice of stimuli depends on the statistical properties of the signal: how easy it is to generate, its noise sensitivity, and for what application the resulting histogram will be used. Some commonly used stimuli are described in the following subsections.

2.4.2 Noise

White Gaussian noise is a wide band signal. In a single characterization run one can thus relate merit figures of the converter to a frequency band. Another benefit for using Gaussian histogram tests (GHTs) is that additional Gaussian distributed measurement disturbance only induces a gain error, which can be circumvented [13, 14].

In [Paper I], a noise stimulus truncated to the working range of the ADC is considered. In order to avoid stimuli outside the working range, the signal is typically generated off-line utilizing a pseudo-random sequence generator. Stimuli values outside the ADC working range are excluded in the sequence [VIII]. An arbitrary signal generator is then used to realize the stimulus samples $s[n]$ for $n = 0, \dots, N-1$, which pdf now can be described as a multidimensional truncated Gaussian pdf.

Let $s[n]$ be an iid distributed realization of a stochastic process. Thus $S = s[n]$ is a stochastic variable with pdf [15]

$$f_S(s) = \begin{cases} \frac{1}{c\sqrt{2\pi\sigma^2}} \exp\left[-\frac{1}{2\sigma^2}(s - \mu)^2\right] & |s| \leq FS \\ 0 & |s| > FS \end{cases}, \quad (8)$$

where the factor c is determined so that $f_S(s)$ integrates to unity, that is

$$c = \int_{-FS}^{FS} \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left[-\frac{1}{2\sigma^2}(s - \mu)^2\right] ds. \quad (9)$$

In (8)-(9), σ^2 is the variance of the Gaussian pdf (before truncation) and μ is its mean value.

2.4.3 Sine Wave

The most commonly used test signal is probably the sine wave [16], due to the ease with which sine waves can be generated and with their spectral purity. The sine wave histogram test (SHT) is a standardized test that is described in the IEEE standard 1241 [8].

One drawback is the (per definition) narrow bandwidth of a sinusoid. Another disadvantage of using SHT is its sensitivity to noise. If noise is present in the stimuli signal, it will modify the probabilities of samples falling in various code bins. The effect of noise will be most significant near the end-points where the curvature of the probability density has its maxima. However, the effect of noise can be made as small as desired by making the signal overdrive large enough.

The pdf of a sine wave is given by

$$f_S(s) = \begin{cases} \frac{1}{\pi\sqrt{FS^2 - s^2}} & |s| \leq FS \\ 0 & |s| > FS \end{cases}. \quad (10)$$

2.4.4 Ramp

Ramp histogram tests are described in the IEEE standard 1241 [8], as well. One advantage of a ramp (or, the triangular wave) over alternative stimuli is that all transition levels of the device under test are equally excited. That is, the input stimulus has a uniform amplitude distribution. Consequently, additive noise will affect all transition levels equally.

The difficulty in generating a satisfactory ramp is a negative aspect of the triangular wave. Due to the nature of the high-frequency content of the ADC testing source, its applicability is restricted to the low and intermediate excitation frequency ranges.

The pdf of a ramp is given by

$$f_S(s) = \begin{cases} \frac{1}{2FS} & |s| \leq FS \\ 0 & |s| > FS \end{cases}. \quad (11)$$

2.4.5 Exponential

The required robustness of testing generators excludes them from being implemented as an embedded block on the ADC chip for purposes such as an automatic diagnostic process. In such a case, an alternative waveform is the exponential signal, which may be generated by discharging a capacitor across the ADC input resistance [17].

The exponential testing signal is easy to generate with required accuracy using a high-quality capacitor. Moreover, the circuitry generating such stimuli is ideally decoupled from any interfering sources and control computer. On the digital side, the test signal is approximated from the ADC data record by the best-fitted exponential

function. However, a low quality capacitor in the generating circuit may result in additional parasitic exponential components in the input stimuli. Experiments reported in [17] show acceptable accuracy of this method for an ADC with 12-bit resolution, and stimuli signal circuitry based on high-quality capacitors commonly available on the market.

In the same way as a sine wave, an exponential stimulus generates a pdf that is sensitive to noise. This is further studied in [18]. The results presented in [18] show that the errors are relatively small and similar to those obtained for a sine wave test. Neither sine waves nor exponential stimuli have superior principally and generally better robustness in relation to additive noise.

The pdf of an exponential stimulus is given by

$$f_S(s) = \begin{cases} -\frac{D}{s - V_{OFF}} & |s| \leq FS \\ 0 & |s| > FS \end{cases}, \quad (12)$$

where

$$D = -\frac{1}{\ln \frac{FS - V_{OFF}}{-V_{OFF} - FS}}, \quad (13)$$

where V_{OFF} is the offset value.

2.4.6 Three-tone

Since it is difficult to generate an appropriate noise signal, a three-tone signal has been used as the stimulus in [Paper III] and [Paper VII]. It is not controversial to claim that the nonlinear order of the ADC can be considered to be at most three. That is, the nonlinearity of the ADC is estimated to be a polynomial of order three. By using a number of three-tone sequences several fundamental, sum and difference products are excited. This stimulus is used to measure Volterra kernels (see Section 3.2) since it excites many points in the volume of the Volterra kernels [19] and in Section 3.5 for the Kautz-Volterra model. The three-tone was also suggested as stimuli for the look-up table [5] in order to get a better coverage in the state-space or phase-plane LUT. The coverage was improved from 75% for a pure sine wave to 93% for the three-tone. However, noise as a stimulus is even better [6] as the coverage was 100%.

For a three-tone scan test scenario, band pass filters are used to suppress spurious noise from the test signal. Inside the filter bandwidth, intermodulation (IM) products, caused in the output stage of the arbitrary generator and the other components in the signal chain, occur. For that reason, the sampling frequency and filter characteristics are chosen so that all interesting distortion products from the ADC (2^{nd} , 3^{rd}

harmonics, and 2nd order IM-products) will fall in the range below the band pass range. The 3rd IM products have frequencies near the three input frequencies and would, hence, not be measurable without further improvements in generating the signals. To overcome limitations of measuring the 3rd order IM products, a pre-distortion was used to obtain spectrally pure three-tone signals for the measurement. Generally, output signals from the generator contain unwanted components (harmonics, IM products and spurs). The idea behind pre-distortion is to add signals to the wanted signals so that the output from the generator will be distortion-free. The implemented method is further described in [20, 21] and is based on iterative algorithms and spectrum analyzer measurements.

2.5 Comparing Different Stimuli

Since the purpose is to characterize a high-speed ADC in a high performance test-bed, the ramp and exponential stimuli are of less importance. However, from a more general point of view it is interesting to study the performance for different stimuli, both existing stimuli and potential future stimuli. The ADC histogram test method is considered as an estimation problem in which the task is to estimate an arbitrary transition level $T[k]$ based on the ADC output. The statistical efficiency of an unbiased estimator can be evaluated by comparing its variance with the corresponding *Cramér-Rao lower bound (CRLB)*, which is an objective estimator performance bound. An estimator that attains the *CRLB* is said to be efficient in that it efficiently uses the data [15]. In [Paper I], the *CRLB* and a minimum variance estimator (MVE) for histogram tests with an arbitrary stimulus were derived.

2.5.1 Cramér-Rao Lower Bound

Assume an arbitrary stimulus $s[n]$ at time instant n , that is $S=s[n]$, where S is a stochastic variable described by its pdf $f_S(s)$. For example (8)-(9) use the truncated Gaussian case. Histogram tests are static and thus the resulting histogram only depends on the amplitude values of the stimulus, and not the order. A Bernoulli model (which is an experiment whose outcome is random and can be either of two possible outcomes) can describe the estimation of a transition level $T[k]$ by histogram tests. It is assumed that the stimulus sequence $s[n]$ for $n=0, \dots, N-1$ is a sequence of iid random variables. The stochastic variable S has a probability p_k of not exceeding T_k , given by the probability distribution function of the stimulus signal. That is $p_k = F(T_k) = \Pr(S \leq T_k)$.

In [Paper I], a minimum variance estimator $g(\hat{p}_k)$ of the transition level $T[k]$ was derived. For a stimulus with a given $F(T[k])$, it was shown that the estimator given in (14) is asymptotically unbiased and optimal in a minimum variance perspective.

$$\hat{T}[k] = g(\hat{p}_k) = F^{-1}(\hat{p}_k). \quad (14)$$

Moreover, the expression (15) is the Cramér–Rao lower bound for unbiased estimators of the transition level $T[k]$, subject to an arbitrary applied stimulus in the histogram test.

$$CRLB(T[k]) = \frac{1}{N} \frac{F(T[k])[1 - F(T[k])]}{f(T[k])^2}, \quad (15)$$

where $f(T[k])$ is the derivative of $F(T[k])$.

The derivation above is for an arbitrary stimulus. In [Paper I], the universal expression in (15) is applied with four different stimuli; sine wave, ramp, noise and exponential, respectively. In [22], [23], and [VIII] the *CRLB* for the special cases sine-wave and Gaussian noise (not truncated) and truncated Gaussian noise were derived, respectively.

The results in [Paper I] are strictly a theoretical comparison between different stimuli. As a complement, [Paper II] presents a metrological comparison between Gaussian and sine-wave histogram tests for wide band applications.

2.5.2 Metrological Comparison of Different Stimuli

The focal point in [Paper II], as well as in the foregoing conference paper [IX], has been to examine to what extent a single characterization by white Gaussian noise can be useful as a characterization over a frequency band as an alternative to several single-tone characterizations. The objective was to evaluate the different stimuli so that the test procedure could be as efficient as possible to find an appropriate characterization for post-correction based on look-up tables. The evaluation is based on measurements on the ADC given in Section 2.3.

The first aim was to characterize nonlinearities in ADCs. The results show that both methods gives reasonable accuracy in characterizing the integral non-linearity. A second aim was to use the obtained information to correct for distortion. By correcting for nonlinearities, the harmonic distortion is supposed to be reduced. However, there is a problem using the error model based on sine wave input signals. The correction is based on a look-up table that is trained for a single frequency only. This will result in inferior performance for signals with other frequencies. Figure 3 illustrates this phenomenon. A 130 MHz sine wave is corrected with a look-up table trained by every tenth megahertz from 120 MHz to 200 MHz. Without any post-correction the *THD* is -71.5 dBc. All models will improve the *THD*, and as expected, the best result is from a model trained on 130 MHz.

In order to study how much the *THD* depends on the training frequency. The outcomes of 81 post-corrected signals are compared in Figure 4. Each of the frequencies 120-200 MHz was used to train a look-up table. Thereafter, new signals from all frequencies are post-corrected. On the x-axis is shown the difference between training frequency and signal frequency. On the y-axis is the improvement in *THD*. A mean value is added to illustrate a trend. However, the number of data is few and it is rather spread. Consequently, the mean value is just a trend and should not be considered as an exact value of improvement.

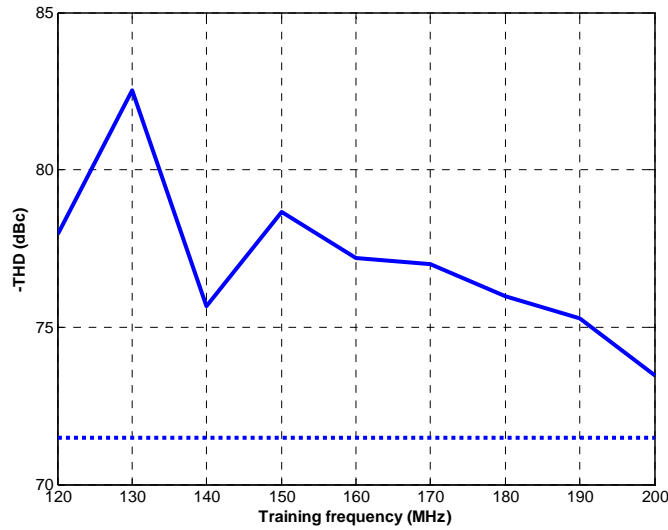


Figure 3: THD for a 130 MHz signal post-corrected by look-up tables trained by frequencies from 120 MHz to 200 MHz (solid line). THD without post-correction (dashed line) is printed as a reference.

As can be seen from the figure the compensation performance is reduced by 4.5 dB when using a model trained by a frequency other than the signal frequency. The model seems to be narrow banded. On the other hand, the distance from training frequency does not seem to be of importance. A similar evaluation is performed in [24] with lower frequencies, and with *SFDR* instead of *THD* as figure of merit. Despite these dissimilarities, both studies point out frequency dependency in the dynamic performance by using this method.

The implication of the above results is that a broadband model is needed to build a look-up table. Two different methods are used and compared to each other and the previously described single-tones models. First, an additional look-up table was trained with all the frequencies, and in such a way to define a broadband model. In Figure 5, the obtained *THD* improvement is compared with the results from the single-tone models. Since their performance is frequency dependent there will be an interval for each frequency. The bars in Figure 5 are intervals in which the upper value is the *THD* improvement from the model trained by the same frequency, and the lowest value comes from the least-fitting model. One may see that the broadband model (solid line) always appears in the upper half of the interval with an improvement of 4-11.5 dB, and it is often close to the top value.

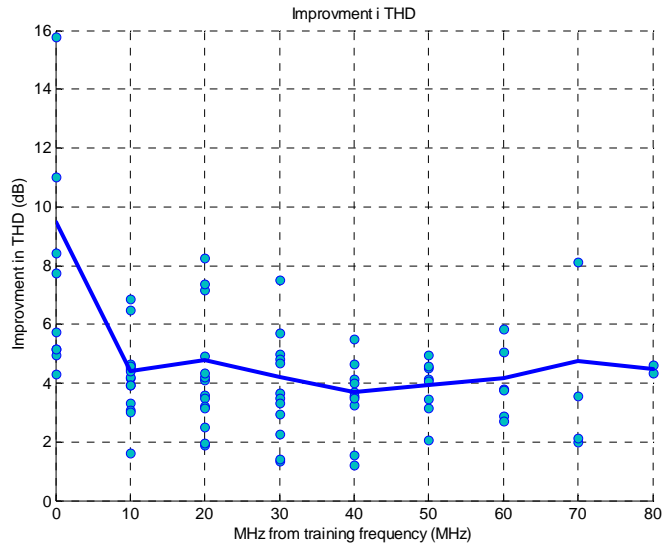


Figure 4: The difference (x-axis) between the training frequency and the actual signal frequency affects the improvement in THD (y-axis). A trend curve (solid line) is used to illustrate the dependency.

Secondly, a look-up table was trained by the noise signal. The evaluation follows the same principle as with multiple single tones and the result is presented as a dashed line in Figure 5. One may note that the performance is inferior compared to the performance of the previous model. In fact, in most cases it does not even reach the performance of the least fitting single tone model. Thus, the preferred stimulus to reduce distortion (*THD*) in wideband application is multiple single tones since the result is superior to Gaussian noise as well as all single-tone characterization

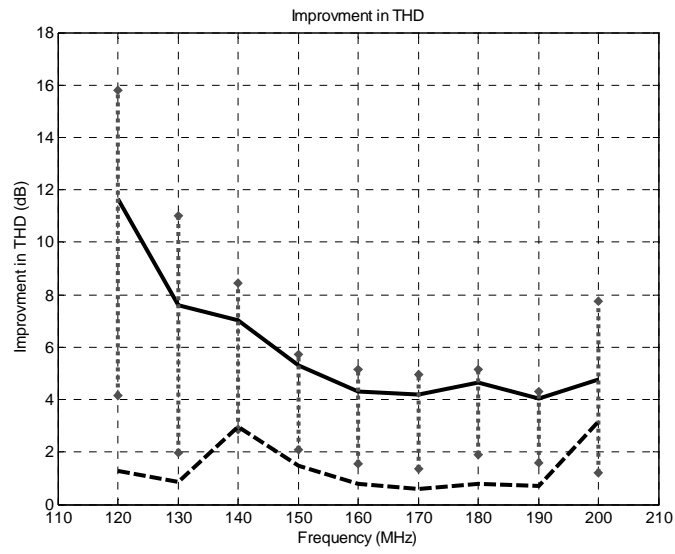


Figure 5: Post-correction based on LUT trained with all frequencies (solid line) and LUT trained with noise (dashed line). The vertical bars are the improvement interval for SHT trained by single frequencies.

3 Models

A model turns out to be useful for investigating the ADC under several operating conditions during the main phases of development: design, evaluation, and improvement. In ADC evaluation, modeling is mainly used to analyze the impact of error sources on the metrological behavior. In ADC improvement, the error occurrence is predicted in a range of operating conditions as wide as possible in order to compensate for error-source effects and correct deterministic errors [25].

Models can be classified according to the abstraction level. Electrical models describe the ADC at the level of electronic components, and a macro model is at a simplified level (such as e.g. Thevenin or Norton-based). Behavior models do not take into account the physical realization of the ADC. The device is characterized by input-output analytic or numerical relations, without going into the depths of the internal structure. Behavioral models are further classified according to their flexibility in: (i) table models, (ii) explicit models and (iii) implicit models.

Table models memorize the input-output characteristic in a look-up table. This strategy turns out to be effective in the verifications following the design, but it is considered to be rigid. In other words, for the specific ADC under analysis, each variation of model parameters requires a new table generation, i.e. minimum flexibility. Moreover, the look-up table implementation requires significant time and memory space.

Explicit models describe the ADC behavior through an analytical relation in a closed form which is easily represented in a programming language. However, this is also their main limitation because easy software packages are not always immediately available. The main advantage of explicit models is the possibility of introducing suitable parameters in the analytic relations to describe different working conditions. This makes the model structure flexible, though it is not easy to leave the specific ADC architecture out of consideration.

An implicit model characterizes the converter either in the time or frequency domain by differential equations with suitable parameters to account for different architectures as well as device classes. They allow the maximum flexibility in the description of the ADC behavior because they can be oriented to the design of a specific converter or a particular architecture. More generally, a whole class of devices can be described by parametrizing the model as a whole and by assigning from time to time the parameter values according to the ADC under analysis.

In behavior modeling the input and output relationship is described as a parametric or non-parametric relation without considering the internal structure of the device under test (DUT). Look-up tables are one example of a non-parametric model, while a polynomial is a parametric model. A model can be either static or dynamic depending on whether the model includes memory effects in the DUT. For an ADC used in RF applications a dynamic model is required. Furthermore, an ADC has a non-linear behavior, so a non-linear dynamic model is required to model an ADC at radio frequency.

There are a large number of available model structures for dynamic non-linear models, such as different kinds of box-models, non-linear feedback, non-linear polynomial state-space [26], Volterra series, or LUTs. The box-models and Volterra will be further described in this chapter.

In this chapter, commonly used dynamic non-linear model will be described in Section 3.1. An ADC has been characterized by measuring the Volterra kernels, which is presented in Section 3.2. In Section 3.3, a dynamic *INL* model is presented, and a method to estimate the model parameters is given in Section 3.4. Finally, the ADC has also been characterized with a Kautz-Volterra model. The results are presented in Section 3.5.

3.1 Dynamic Nonlinear Models

3.1.1 Dynamic Look-up Tables

ADC post-correction using LUT was the first method proposed besides dithering. There are two different types of tables that are considered: the phase-plane [7] and state-space [5, 6]. In a phase-plane approach, the error is related to the amplitude and slope of the input. For the state-space approach, the error is related to the current sample amplitude and the previous sample amplitude. In [3, 27], a further development of the state-space method is suggested in which a generalized approach is taken with full flexibility between the dynamics (that is, the number of delayed samples) and the precision of each sample. Thus, the size of the multidimensional look-up table is kept at a reasonable, predetermined number. However, these methods are burdensome considering the time it takes to train the entries of the LUT as well as the requirement on the memory size.

3.1.2 Volterra Models

Volterra theory can be used to describe causal nonlinear time invariant dynamic systems with fading memory [28]. The Volterra series can be said to be a “Taylor series with memory” and Volterra theory is applicable in systems in which the nonlinearities are small compared to the linear term. Time-domain Volterra models have been used for modeling ADCs (e.g. [29]) and for ADC post correction (e.g. [30]). The Volterra series describes the relation between the system’s input $v[t]$ and the system’s output $y[t]$ as

$$y[t] = \sum_{n=0}^{\infty} y_n[t], \quad (16)$$

where

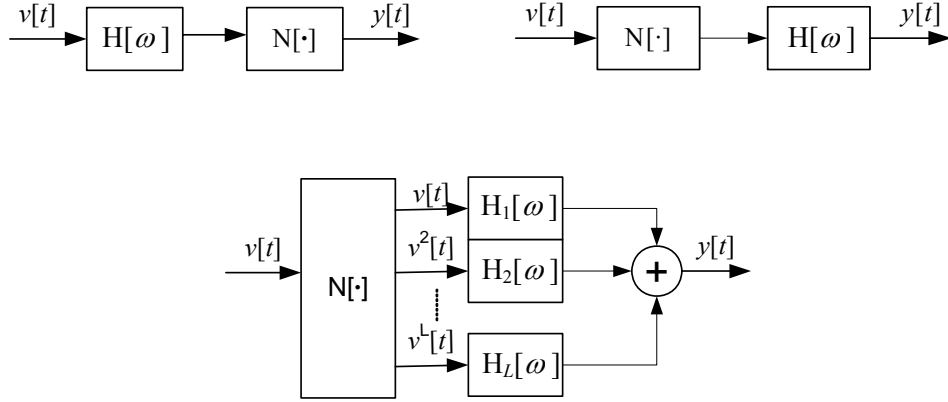


Figure 6: Block diagram representations of: (a) the Wiener model (upper left), (b) the Hammerstein (upper right), and (c) the parallel Hammerstein model.

$$y_m[t] = \int \cdots \int h_i[\tau_1, \dots, \tau_i] v[t - \tau_1] \cdots v[t - \tau_i] d\tau_1 \cdots d\tau_i, \quad (17)$$

with $h_i[\tau_1, \dots, \tau_i]$ being the i -th order time domain Volterra kernel. The i -th order frequency domain Volterra kernel, $H_i[s_1, \dots, s_i]$, is obtained by the Laplace transform of $h_i[t_1, \dots, t_i]$.

A couple of drawbacks of Volterra models are the high number of parameters and the involved computational complexity. To deal with these difficulties, special cases of the Volterra model, such as Hammerstein and Wiener box models, are thus used, although they do not have the general properties of a Volterra model.

An extension of the Volterra model is to use of a Kautz-Volterra (KV) model to characterize an ADC. The model uses orthonormal basis functions, or so-called Kautz functions [31]. The KV model has the same general properties as the Volterra model, but the number of parameters can be significantly lower. A Volterra model is based on FIR filters; a KV model uses IIR filters and in practice can be used for systems with longer memory effects [32]. Kautz-Volterra models have been successfully used for modeling power amplifiers [33, 34] and for digital pre-distortion [34, 35].

3.1.3 Box Models

Two commonly used box models to describe a dynamic nonlinear system are the Wiener-model and the Hammerstein-model. Both methods separate the dynamics from the nonlinearity. A Wiener model is represented by a linear filter $H[\omega]$ followed by a static nonlinearity $N[\cdot]$ see Figure 6a. The Hammerstein model is given by the same two blocks but in the opposite order, see Figure 6b. The parallel Hammerstein model is an extension of the ordinary Hammerstein model as depicted in Figure 6c. The difference between the ordinary model and the parallel structure is that the contributions of different orders ℓ are now filtered by different filters, $H_\ell[\omega]$, respectively.

The models developed in this thesis are built on discrete time signals. Thus, the frequencies used are

$$\omega = 2\pi \frac{f}{f_s}, \quad (18)$$

where f is the absolute frequency and f_s is the sampling frequency. However, some results are presented as function of the absolute frequency.

3.2 Measuring Volterra Kernels

[Paper III] and the foregoing conference paper [XII] describe how frequency domain Volterra kernels of an ADC are determined. Memory effects are seen as frequency dependence, and the frequency domain Volterra kernels, thus, are measures of nonlinear memory effects. The Volterra kernels were determined using a technique in which the ADC is excited with three-tone signals. The technique is similar to previously reported ones [36, 37]. In [36, 37], a multi-tone signal was used, which has the advantage that the Volterra kernel is determined in many points simultaneously. The frequencies of the multi-tone signals must be chosen with care; Volterra kernels of different orders cannot have output signals with components at the same frequency. A disadvantage of using multi-tone signals is that the peak-to-RMS ratio of the signal is high. This is particularly undesirable in ADC testing. The reason is that an ideal test signal for ADCs excites all transition levels equally. However, this can be resolved by adjusting the phase for the different tones to achieve a lower peak-to-RMS ratio [38]. Instead a number of three-tone signals were used, where each three-tone signal has a unique set of frequencies for the three tones.

The sampling frequency was close to 175 MHz and the signal frequency range was 63.6 - 74.7 MHz. Two frequencies were kept constant – one close to 67.0 MHz and one close to 70.9 MHz. The third one was stepped in the given frequency range. These frequencies result in trajectories on two surfaces in the f_1, f_2 – plane: one surface for harmonics and one for IM – products.

The results show no obvious relations between $H_1[f]$ and $H_2[f_1, f_2]$, and the latter has a more pronounced frequency dependence, while the former show insignificant frequency dependence. In other words the memory effects of the linear term and those of the 2nd order term are of different character.

Nonlinear response functions can be described by networks of static nonlinearities and linear filters [39]. Different box models (see Section 3.1.3) give Volterra kernels of different symmetry. We analyze the symmetry of the $H_2[f_1, f_2]$ and compared the measured results with the expected symmetries from Wiener and Hammerstein block models. The determined $H_2[f_1, f_2]$ of the ADC has, the symmetry properties of a Hammerstein system. However, when comparing the second order Volterra kernel $H_2[f_1, f_2]$ with the first order Volterra kernel $H_1[f]$. The linear filter of $H_1[f]$ and $H_2[f_1, f_2]$ cannot be the same. We therefore suggest a parallel Hammerstein model for the tested ADC, as shown in Figure 6c.

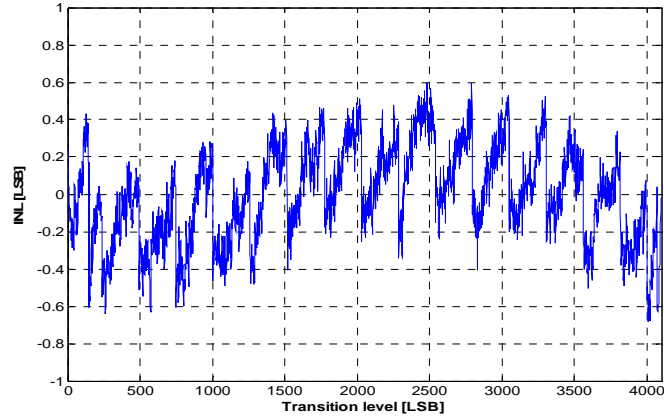


Figure 7: Exemplary measured INL from a 12 bit commercial ADC.

3.3 Dynamic INL Modeling for ADC Characterization

Based on the promising results in Section 3.2, employing a parallel Hammerstein model on ADC characterization by [Paper III], the model will be used throughout this section in order to analyze and compensate for the nonlinear dynamic parts of ADC integral nonlinearity. Note that the linear filter $H_1[\omega]$ can be considered as constant, which corresponds to the gain G in (2). The *INL* is defined after correction for gain and offset, thus a dynamic *INL* –model may be found from the parallel Hammerstein model where the linear filter $H_1[\omega]$ is excluded.

However, in order to fully describe the behavior of a nonlinear system using Volterra kernels or a box-model, the transfer function must be continuous, which is generally not true for an ADC (see e.g. Figure 7). Thus, an alternative representation is needed.

In Figure 7, a typically measured *INL* from a commercial ADC is plotted. As is evident from the plot, the behavior is a combination of a smooth wave or polynomial curve and a prickly saw-tooth wave. In the following analysis, the *INL* will be broken up in two components; one represents the smooth curve and one represents the prickly saw-tooth wave. The *INL* is then described as

$$INL[k] = {}^{HCF}INL'[k] + {}^{LCF}INL[k], \quad (19)$$

where the first term is the contribution by the, so called high code frequency component and the second term by the low code frequency component. In [40], the static *INL* model was expressed as a one dimensional image in the code k domain consisting of the two components. The smooth curve was called a low-code

frequency, LCF ¹ [41] component ($^{LCF}INL[k]$) and was represented by a polynomial approximation:

$$^{LCF}INL[k] = h_0 + h_1k + h_2k^2 + \dots h_Lk^L, \quad (20)$$

where the h_k 's are the polynomial coefficients and L is the order of the polynomial. The parameters h_0 and h_1 are typically set to zero due to the fact that INL is calculated after a correction has been made for gain and offset errors [8]. The high code frequency component ($^{HCF}INL[k]$) is caused by a significant deviation from the mean value of the differential nonlinearities. In [XIII], the high code frequency component was further divided into two parts – $^{HCF}INL[k]$ and $^{Noise}INL[k]$, respectively. The former term, $^{HCF}INL[k]$ (hereafter denoted HCF), depends on the physical design of the component (designs such as pipeline, successive approximation or any other structure) and is modeled as piecewise linear [40] [XIII]. The latter component, $^{Noise}INL[k]$, is the part of INL that can not be described by an equation. Thus, the INL model in (19) is refined to

$$INL[k] = ^{HCF}INL[k] + ^{LCF}INL[k] + ^{Noise}INL[k]. \quad (21)$$

A static model of an ADC and in particular the corresponding $INL[k]$ is in general not sufficient to accurately describe an ADC in a wideband application. Hence, the dynamic behavior also needs to be included in the model, which can be done by adding amplitude information from either previous sample amplitudes or estimates of the input slope (state-space and phase-plane modeling, respectively). In the present work, a frequency dependent INL model is employed. The dynamic behavior of the INL can alternatively be described as a frequency dependency; that is, different sine wave test stimuli result in different INL data. The measurement span over the test frequencies in a grid $\{f_1, \dots, f_M\}$. The frequency variable will be denoted by the variable m ($m = 1, \dots, M$). In order to stress the dependency of some of the components in (21) on the stimuli frequency (21) is rewritten as

$$INL[k, m] = ^{HCF}INL[k] + ^{LCF}INL[k, m] + ^{Noise}INL[k, m]. \quad (22)$$

The main purpose of the model (22) is to use it for post-correction. The structure of the components of the model may, to some extent, be affected by the goal of finding a dynamic model that is easy to train and simple to implement. Even though the behavior models are black box models, the arguments for having a static HCF can be justified based on some knowledge of the ADC design. The hardware structure of an ADC consists of two sections. First is an analog signal processing section with an

¹ To understand the meaning of low frequency code, consider that the code axis represents a time axis. Accordingly, low-code frequency means slow variation over the codes.

amplifier and sample-and-hold circuits followed by a section that performs quantization. The high code frequency component, HCF , mainly represents the imperfections in the quantizer, which are (at least in a first approximation) static and thus depend on the code k only and not on the test frequency. One favorable feature of considering the high code frequency component to be static is that the size of the look-up table will be minimized. The low code frequency component, LCF , is a parametric model. Hence, it can be compensated by computations.

The LCF is described as a nonlinear dynamic model. The linear term shows no frequency dependence, thus the filter frequency function $H_1[\omega]$ can be considered as a constant for an ADC. Note that with $H_1[\omega]=h_z$, the parallel Hammerstein model reduces to the polynomial model in (20).

In order to fully describe the behavior of a nonlinear system using Volterra kernels or a box-model, the transfer function must be continuous, which is generally not true for an ADC (see e.g. Figure 7). However, the LCF is a continuous function by construction. Moreover, LCF is the dynamic component in the INL -model. Thus, a parallel Hammerstein model is suitable as a model structure for LCF , while the non-continuous behavior is modeled by the remaining HCF and $^{Noise}INL[k,m]$, respectively. The complete block scheme is given in Figure 8. The high code frequency component HCF depends on the code k only, and not on the test frequency. Further, HCF is, as in [Paper VI], assumed to be piecewise linear in the code k ; in other words, it is described by the first order polynomial $\alpha_0+\alpha_1k$ within a limited set of neighboring code values $k_{p-1} \leq k < k_p$, which is denoted as the code interval K_p . The $^{HCF}INL[k]$ is thus modeled such that

$$^{HCF}INL[k] = \alpha_0[p] + \alpha_1[p](k - k_{p-1}), \quad (23)$$

where p refers to the ordered code interval

$$K_p : \{k | k_{p-1} \leq k < k_p\}, \quad (24)$$

where $p = 1, \dots, P$. The initial value of k_0 is given by $k_0 = 1$, and the upper end point is, by definition, $k_p = 2^N$. Typically, the number of intervals P is small compared with the total number of codes, $P \ll 2^N - 1$; see, for example, the INL curve given in Figure 10.

Two different post-correction methods based on the theories given in this section were presented in [42] and [XIII], respectively. In both papers the different components, LCF and HCF , were post-corrected separately and the dynamics were concentrated to the low-code frequency component.

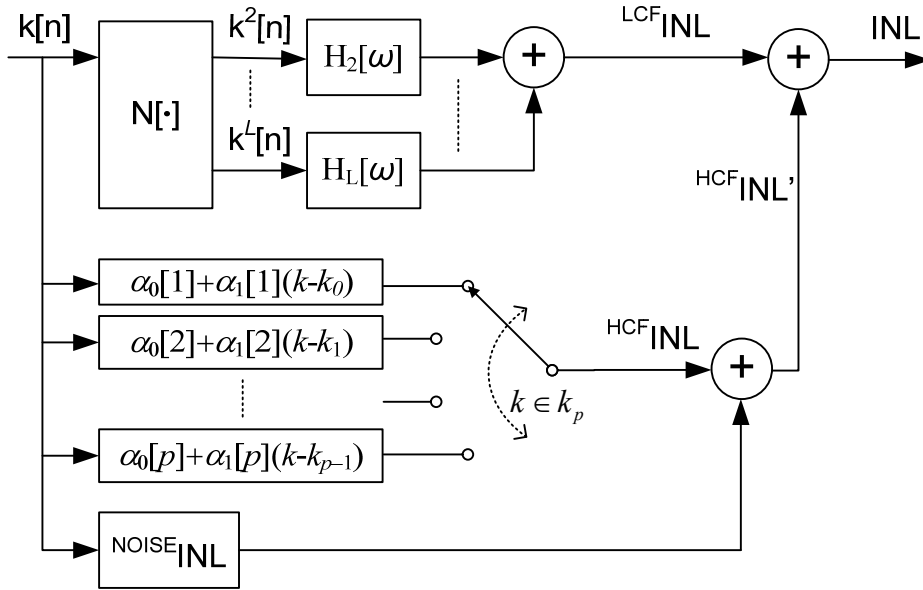


Figure 8: A block scheme over the complete INL model. The non-linear block $N[\cdot]$ is a polynomial.

In [XIII] the magnitude response for the two filters $H_2[\omega]$ and $H_3[\omega]$ were plotted (see Figure 9) for the ADC used. The results are based on simulation. The ADC is characterized over the frequency range 10 – 90 MHz, which gives an 80 MHz bandwidth, which is slightly less than 80 % of the Nyquist frequency. From the figures it is clearly observable that the parameters obtain a frequency dependency, similar to a second order system with complex-valued roots. From Figure 9, one may note that the magnitude of the coefficients increases at frequencies above 70 MHz. This is in accordance with the data sheet, where the $SFDR$ starts to decrease at that frequency.

The HCF is estimated to be piecewise linear. The code intervals K_p are chosen manually from the graph in Figure 10.

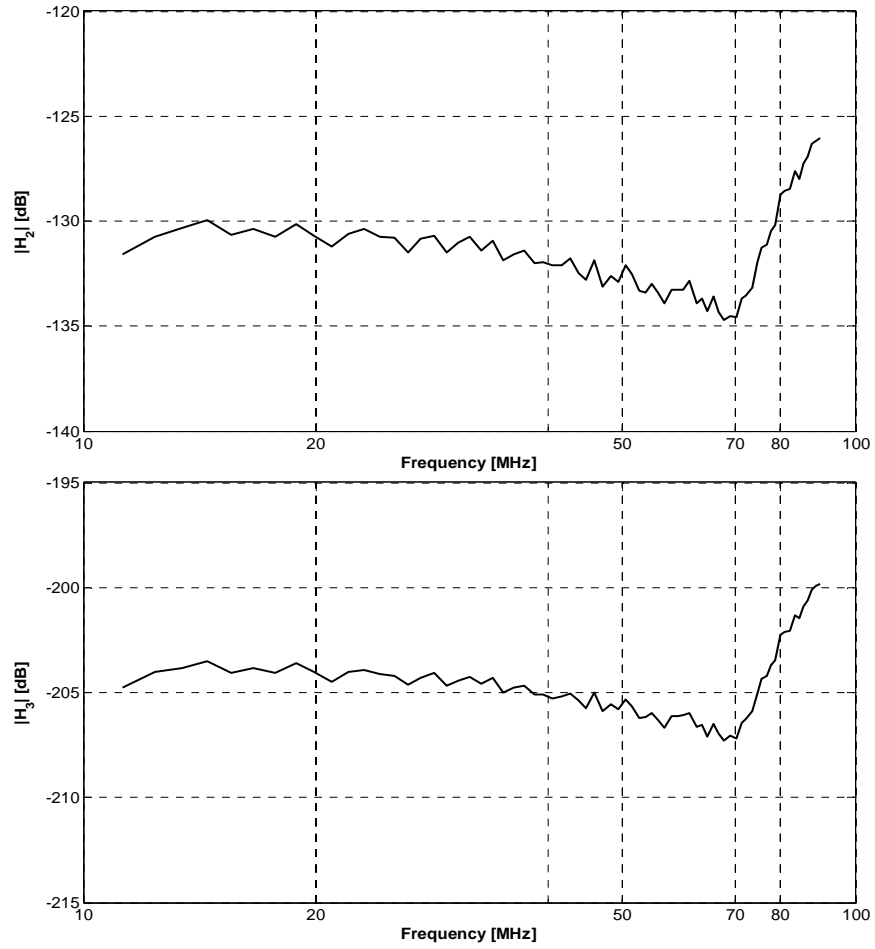


Figure 9: The magnitude response from filters $H_2[f]$ and $H_3[f]$

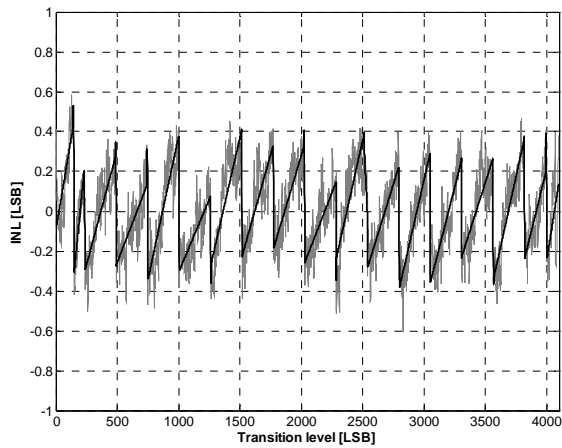


Figure 10: The $\text{HCF} \text{INL}[k]$ (black line) is estimated from the $\text{HCF} \text{INL}'[k]$ (grey line), which is a combination of $\text{HCF} \text{INL}[k]$ and $e[k]$

3.4 A Closed Form Solution to the Estimation Problem

In [Paper VI] and [XV], the dynamic characterization of an ADC, when using a plurality of test frequencies in the measurement set-up, was considered. The *LCF* and *HCF* are parameterized and a least-square method was derived for the estimation of the parameter values from the obtained measurements. A closed form solution to the estimation problem was derived. The *HCF* is assumed to be piecewise linear in the code k , that is described by (23) and (24). Accordingly, there are P sets of polynomial coefficients $\{\alpha_0[p], \alpha_1[p]\}$, which are gathered in the parameter vector η of size $2P$. That is,

$$\eta = \begin{pmatrix} \alpha_0[1] \\ \alpha_1[1] \\ \vdots \\ \alpha_0[P] \\ \alpha_1[P] \end{pmatrix}. \quad (25)$$

The parameter vector η in (25) describes the local gain and offset in *INL* for the different code intervals K_p . As previously mentioned, this part of modeling the *INL* is, at least approximately, independent of the input test frequency. The *LCF* models the remaining dynamic behavior of the *INL*. The *LCF* is modeled by a polynomial of order L (20). Consider the signal model

$${}^{LCF}INL[k, m] = f[k]^T \theta[m], \quad (26)$$

where T denotes transpose. In (26), the vector $\theta[m] = (h_0[m] \cdots h_L[m])^T$ is the parameter vector (that is, $\theta[m]$ is possibly dependent on the test frequency as indicated by the argument m) and $f[k] = (1 \ k \ \cdots \ k^L)^T$ is the regressor. For a single set of *INL*-data obtained for an arbitrary test frequency f_m determined by the integer m

$$\mathbf{y}_m = \begin{pmatrix} INL[1, m] \\ \vdots \\ INL[2^N - 1, m] \end{pmatrix}. \quad (27)$$

We introduce (where p spans $p=1, \dots, P$)

$$\mathbf{g}_p = \begin{pmatrix} 1 & 0 \\ \vdots & \vdots \\ 1 & k_p - k_{p-1} - 1 \end{pmatrix}, \quad (28)$$

with the convention that $k_0 = 1$ and $k_p = 2^B$. Further, introduce the Vandermonde matrix \mathbf{f} of size $2^N - 1 \times L + 1$ given by

$$\mathbf{f} = \begin{pmatrix} 1^0 & 1^1 & \dots & 1^L \\ \vdots & \vdots & & \vdots \\ (2^B - 1)^0 & (2^B - 1)^1 & \dots & (2^B - 1)^L \end{pmatrix}. \quad (29)$$

Then we may put the *INL* on a vector form as

$$\mathbf{y}_m = \mathbf{g}\eta + \mathbf{k}\theta[m] + \mathbf{e}_m, \quad (30)$$

where η is given by (25), respectively. Here, \mathbf{g} is introduced as the block diagonal matrix with the \mathbf{g}_p 's defined by (28) on its main diagonal, that is $\mathbf{g} = \text{blockdiag}(\mathbf{g}_1, \dots, \mathbf{g}_p)$.

For M sets of test frequencies we have to augment the model in (20) by incorporating the multiple data sets $\{\mathbf{y}_1, \dots, \mathbf{y}_M\}$ and expanding the parameter vector with the m -dependent components, that is

$$\underbrace{\begin{pmatrix} \mathbf{y}_1 \\ \vdots \\ \mathbf{y}_M \end{pmatrix}}_{\mathbf{y}} = \underbrace{\begin{pmatrix} \mathbf{g} & \mathbf{f} \\ \vdots & \ddots \\ \mathbf{g} & \mathbf{f} \end{pmatrix}}_{[\mathbf{GF}]} \underbrace{\begin{pmatrix} \eta \\ \theta(1) \\ \vdots \\ \theta(M) \end{pmatrix}}_{\begin{bmatrix} \eta \\ \theta \end{bmatrix}} + \underbrace{\begin{pmatrix} \mathbf{e}_1 \\ \vdots \\ \mathbf{e}_M \end{pmatrix}}_{\mathbf{e}}. \quad (31)$$

The least squares (LS) solution is given by

$$\begin{bmatrix} \hat{\eta} \\ \hat{\theta} \end{bmatrix} = \left(\begin{bmatrix} \mathbf{G}^T \\ \mathbf{F}^T \end{bmatrix} \begin{bmatrix} \mathbf{G} & \mathbf{F} \end{bmatrix} \right)^{-1} \begin{bmatrix} \mathbf{G}^T \\ \mathbf{F}^T \end{bmatrix} \mathbf{y}. \quad (32)$$

In [Paper VI], it is shown that the above LS solution can be separated into one solution for η and one for θ . Moreover, the complexity of the LS solution is significantly reduced by exploiting the spares structure of the involved matrices.

$$\hat{\boldsymbol{\eta}} = (\mathbf{g}^T \boldsymbol{\pi}_\perp \mathbf{g})^{-1} \mathbf{g}^T \boldsymbol{\pi}_\perp \bar{\mathbf{y}}. \quad (33)$$

$$\hat{\theta}_{[m]} = (\mathbf{f}^T \mathbf{f})^{-1} \mathbf{f}^T (\mathbf{y}_m - \mathbf{g} \hat{\boldsymbol{\eta}}), \quad (34)$$

where

$$\bar{\mathbf{y}} = \frac{1}{M} \sum_{m=1}^M \mathbf{y}_m, \quad (35)$$

$$\boldsymbol{\pi}_\perp = I - \mathbf{f} (\mathbf{f}^T \mathbf{f})^{-1} \mathbf{f}^T. \quad (36)$$

We note that (33) is a linear combination of the sum of the data. Regarding (34), one may note that this is the least-squares solution to the de trended data $\mathbf{y}_m - \mathbf{g} \hat{\boldsymbol{\eta}}$.

3.5 The Kautz-Volterra Model

Volterra filters are simple to use and have nice properties. For example, they are linear in the parameters, and thus standard and well-behaved parameter estimations techniques can be applied. However, the need of intensive computational schemes limits their practical use. This is mainly due to the slow convergence of a huge number of coefficients that must be estimated in order to calculate the kernels. The output $y_V(n)$ of a discrete-time time-invariant truncated O -th order and memory length M Volterra model with input sequence $v(n)$ is

$$\begin{aligned} y_V(n) &= \sum_{m=0}^M h_1(m) v(n-m) \\ &+ \sum_{m_1=0}^M \sum_{m_2=m_1}^M h_2(m_1, m_2) v(n-m_1) v(n-m_2) + \dots, \quad (37) \\ &+ \sum_{m_1=0}^M \dots \sum_{m_O=m_{O-1}}^M h_O(m_1, \dots, m_O) v(n-m_1) \dots v(n-m_O) \end{aligned}$$

where $h_i(m_1, \dots, m_i)$ are the i -th order time domain Volterra kernels. The i -th order frequency domain Volterra kernel $H_i[z]$ is obtained by the Laplace transform of $h_i(m_1, \dots, m_i)$. Thus, the $H_1[z]$ is a linear FIR filter, $H_2[z]$ is a quadratic FIR filter, *et cetera*. Previous work such as [32], interprets (37) as a filter bank of $M+1$ linear filters (filter i is defined as $G_i[z] = z^{-(i-1)}$) followed by an $M+1$ input, static nonlinear Volterra system. In order to reduce the number of coefficients caused by high model order O and memory length M the Kautz-Volterra model pre-filters the input signal $v(n)$ with orthonormal IIR filters, where the poles are chosen according to *a priori*

knowledge of the system properties. By judicious choice of the filters, a model with good accuracy can be achieved with a small number of basis functions. The KV model of order O is defined as

$$y_{KV}(n) = \sum_{j=1}^{J_1} b_j x_{1,j}(n) + \sum_{j_1=1}^{J_2} \sum_{j_2=j_1}^{J_2} b_{j_1 j_2} x_{2,j_1}(n) x_{2,j_2}(n) + \dots$$

$$+ \sum_{j_1=1}^{J_O} \sum_{j_2=j_1}^{J_O} \dots \sum_{j_O=j_{O-1}}^{J_O} b_{j_1 j_2 \dots j_O} x_{O,j_1}(n) x_{O,j_2}(n) \dots x_{O,j_O}(n)$$
, (38)

where J_1 is the number of basis functions for order 1, *et cetera*, and $x_{i,j}(n)$ is the i -th nonlinear order output of the filter $G_{i,j}$ excited by input signal $v(n)$.

$$G_{i,j}(z) = \sqrt{[1 - (\xi_j \xi_j^*)^2][1 - \delta_j^2]} \frac{z}{(z - \xi_j)(z - \xi_j^*)} \prod_{q=1}^{j-1} \frac{(1 - \xi_q z)(1 - \xi_q^* z)}{(z - \xi_q)(z - \xi_q^*)}, \quad j \text{ odd}$$

$$G_{i,j}(z) = \sqrt{1 - (\xi_j \xi_j^*)^2} \frac{z(z - \delta_j)}{(z - \xi_j)(z - \xi_j^*)} \prod_{q=1}^{j-1} \frac{(1 - \xi_q z)(1 - \xi_q^* z)}{(z - \xi_q)(z - \xi_q^*)}, \quad j \text{ even}$$

$$j = 1, 2, \dots, J$$

$$\delta_j = (\xi_j + \xi_j^*) / (1 + \xi_j \xi_j^*)$$

(39)

where ξ_q and ξ_q^* are the complex-conjugate poles-pairs of order i .

The notation $\mathbf{J}=[J_1 J_2 J_3]$ is used for the number of basis functions of the respective order in the experiments and denote the poles $\boldsymbol{\xi}=[p_1, p_2, p_3]$. The KV model could be used with several poles per order (see (39)); here, one complex pole-pair per nonlinear order is used. If all the poles are at the origin ($\boldsymbol{\xi}=[0 \ 0 \ 0]$), the KV model becomes the Volterra model, and if $\mathbf{J}=[1 \ 1 \ 1]$, it becomes a polynomial model [34]. For the ADC under test a third-order model is used.

If the poles in $\boldsymbol{\xi}$ are known, the constants $b_l \dots$ can be identified from $v(n)$ and the experimental output $y(n)$, using standard techniques for system identification, i.e. minimizing the mean square error of the experimental and model outputs e.g. [43, 44]. The optimum poles, in a mean square error sense, were found as follows. First, determined p_1 was determined with the quadratic and cubic set to zero; then, p_1 were fixed and p_2 was determined with only the cubic term equal to zero; and finally p_3 were determined with p_1 and p_2 fixed.

Three-tone signals (Section 2.4.6) were used as input signals, $v(n)$, for identification. The sampling frequency was close to 175 MHz (174997504 Hz) and the signal frequency range was 63.6 - 74.7 MHz.

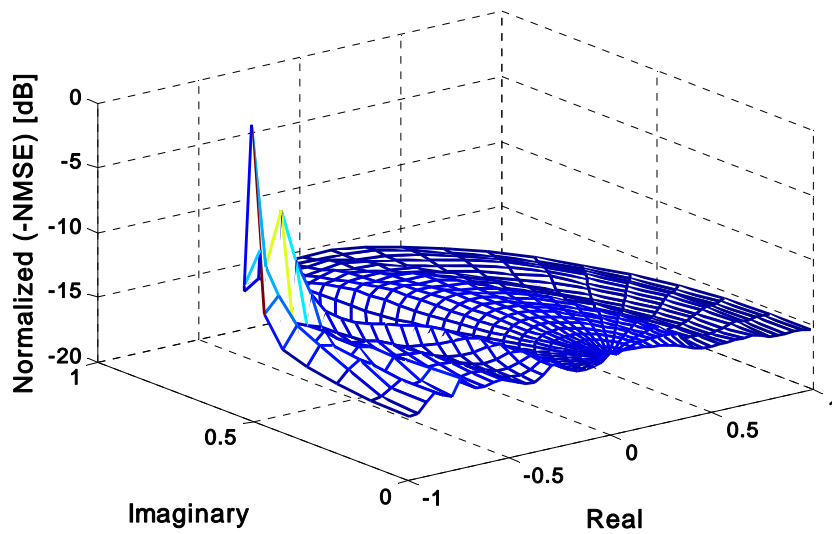


Figure 11: Show variations in the NMSE due to the position of the third-order pole placement. The optimal placement of the pole was found at $-0.7 \pm 0.7j$ and gave an NMSE of -50.3 dB (here normalized to 0). The identification of the KV model was performed based on a three-tone signal at fixed frequencies.

The results are based on twenty independent sets of three-tone signals as input signals. For the linear and second order non-linearity, the dynamic effect was negligible; but for the third order nonlinearity the improvements was significant. The optimal pole placements were found close to the unit circle. In Figure 11, the pole placement for a single set of three-tone stimulus is shown. The optimal placement of the pole was found at $-0.7 \pm 0.7j$, which implies a resonance frequency at 65.6 MHz. In [XIII], similar results were achieved when the same ADC was characterized by a single-tone signal with a step-wise increased frequency as stimuli (see Chapter 3.3).

It was also shown that the optimal pole placement can be considered to be frequency independent in the used bandwidth.

A choice of the ordinary Volterra model, i.e. choosing $\xi=[0 \ 0 \ 0]$, would have resulted in a more complex model structure compared to the proposed structure due to a higher memory length.

4 Model-Based Post-Correction

Post-correction can be divided into two different methods. One method is to use an inverse model and the other is to add a correction term. When using LUT for post-correction the two methods are often denoted *replacement* and *correction*, respectively. The inverse model corresponds to replacement. The output code from the ADC is a table index. The code addresses a memory where the memory value of that address is an estimate of the analog input. The index can also be compounded by one or more previous samples (see Figure 12). If the current and previous samples together constitute an address in the correction table, it is called state-space correction. If the current and the difference between the current and previous sample (the slope) constitute an address, it is called phase-plane. Also, a more complex alternative has been presented [3, 27].

Figure 12 can also represent a correction method based on inverse models. In other words, the method is based on some mathematical system model and its inverse. Typically, a model is characterized for the DUT. The model gives an approximation of the input-output signal relationship. An inverse – possibly approximate – of the model is calculated thereafter. The model inverse is used in sequence after the ADC, hence operating on the output samples, in order to reduce or even cancel the unwanted distortion.

Instead of replacing the output code from the ADC, one can add a correction term. See Figure 13. In post-correction using LUT, the output sample (possibly together with previous samples) addresses a correction term instead of an estimate of the input as in the replacement method. The correction term is added to the output code. In model based post-correction, the post-correction term is computed from a mathematical model. The correction term is added to the output code. In a static post-correction, the correction term corresponds to the *INL*.

The outline of this chapter is as follows. In Section 4.1, it will be explained how the models obtained in Chapter 3 can be used for post-correction. Further, in Section 4.2, the maximum achievable performance improvements for a model-based post-correction are presented.

4.1 Post-Correction Based on Parametric Models

The choice of post-correction method is dependent on the ADC modeling. A model designed to express the input-output relation of the full ADC is suitable for a post-correction based on an inverse model, while a model describing the deviation in output code between a practical and ideal ADC is intended to perform post-correction by adding a correction term.

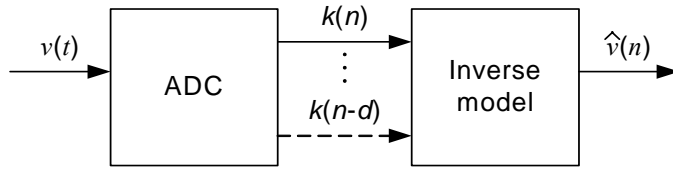


Figure 12: Post-correction by using an inverse model of the ADC.

Two appended papers [Paper III, Paper VII] model the behavior of the full ADC. These models can thus be used to generate an inverse model, which will be used in sequence after the ADC. However, when generating an inverse model of a dynamic nonlinear system, the memory depth of the inverse will be longer than the direct model, or truncated. An alternative method is to identify the inverse model directly, which is done in e.g. [45].

The Kautz-Volterra model, in [Paper VII], has properties that are favorable for generating inverse models. It is shown [46] that small memory effects in the linear term cause the poles of inverse and direct models to be the same. Consequently, the KV model might be particularly suitable for post-correction by using an inverse model. However, until today, no results have been published based on an inverse KV-model post-correction.

The [Paper III], the measured Volterra model was compared with different box-models, where the parallel Hammerstein model was the preferred model. The Volterra model itself has not been aimed for post-correction. Instead, the parallel Hammerstein model has played an important role in building an error model of the ADC aimed for error correction. In addition to the parallel Hammerstein model, complementary components used to describe non-continuous behavior are used in the full ADC error model (see Section 3.3). The approach is to build an error model of the ADC, and estimate a correction factor to be added to the ADC output to cancel the unwanted distortion by Figure 13.

4.2 Performance Analysis

The purpose of post-correction is to improve the performance for a system in which ADCs are used. Commonly used figures of merit are *THD*, *SFDR*, and *SINAD*. For a model-based post-correction based on the model structure described in the previous section, and given that all model parameters are estimated, questions of relevance include: What are the achievable performance improvements for these figures of merits? How advanced must the post-correction method be to meet the demands for the system?

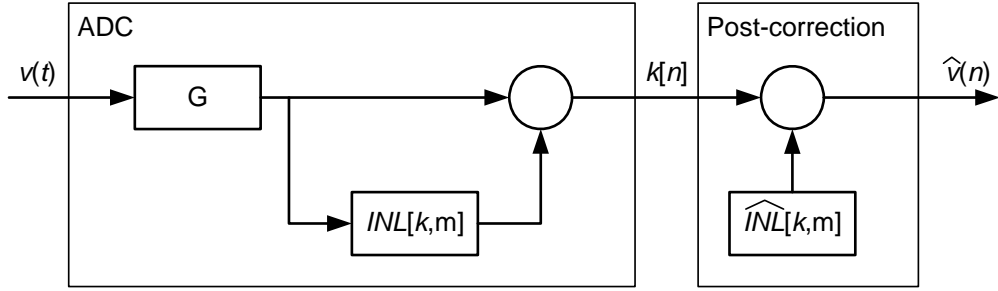


Figure 13: Post-correction of an ADC by adding a correction term. The block G includes analog pre-processing, sample and hold, and quantization.

In the following section the relationship between a given INL -model and the ADC performance is formulated, and, hence, the potential of improvement of an optimal post-correction. Below, the influence of the three terms in (22) on the ADC performance measures are investigated separately. By gradually correcting for each INL -term the performance will improve step by step. We consider the case when a multi-term dynamic model of the INL (such as (22) above) is available, and is used for post-correction.

The term $^{Noise}INL[k,m]$ in (22) is modeled as noise throughout the thesis so that $^{Noise}INL[k,m] = e[k,m]$ is assumed to be zero mean independently identically distributed noise both in the code k and in input frequency m . The general relation (22) is accordingly reduced to

$$INL[k,m] = {}^{LCF}INL[k,m] + {}^{HCF}INL[k] + e[k,m]. \quad (40)$$

In [Paper IV], the different components are described in more detail, as well as how they affect the performance of the ADC. For a given INL , static or dynamic, the performance (such as THD and $SINAD$) of the ADC will be affected. Using post-correction can minimize the amplitude deviation, and thus improve the performance of the ADC. In the following section the relation between a given INL -model and the ADC performance is summarize, and, hence, the potential of improvement of an optimal post-correction. Below, the influence of the three terms in (40) on the ADC performance measures are investigated separately. By gradually correcting for each INL -term the performance will improve step by step.

The low-code frequency component is a weakly non-linear dynamic transfer function given by the block diagram in Figure 6c. Since its transfer function is a polynomial, LCF will mainly affect the harmonic distortion such as THD , but also $SFDR$ since the 2nd and 3rd harmonics are usually the limiting spurs in $SFDR$. To get a measure on how the ADC performance depends on this component, an evaluation in the frequency domain is done.

For simplicity, but without loss of generality, the analyses are performed in continuous time. Let the time domain input $v[t]$ to a static nonlinear system be a unit amplitude cosine

$$v[t] = \cos 2\pi f_0 t = \frac{e^{j2\pi f_0 t} + e^{-j2\pi f_0 t}}{2}. \quad (41)$$

where t is the absolute time. The harmonic distortion on the output $x[t]$ of a static nonlinearity like the *LCF* driven by input $v[t]$ is given by a combination of (41) and (20). That is

$$x[t] = h_0 + h_1 \frac{e^{j2\pi f_0 t} + e^{-j2\pi f_0 t}}{2} + h_2 \left(\frac{e^{j2\pi f_0 t} + e^{-j2\pi f_0 t}}{2} \right)^2 + \dots + h_L \left(\frac{e^{j2\pi f_0 t} + e^{-j2\pi f_0 t}}{2} \right)^L. \quad (42)$$

The even exponents produce harmonic distortion products at the DC level and on even multiples of the fundamental frequency. Odd exponents will result in distortion at odd over-tones. For example the third order component reads

$$\begin{aligned} h_3 \left(\frac{e^{j2\pi f_0 t} + e^{-j2\pi f_0 t}}{2} \right)^3 &= h_3 \left(\frac{e^{j3 \cdot 2\pi f_0 t} + e^{-j3 \cdot 2\pi f_0 t} + 3(e^{j2\pi f_0 t} + e^{-j2\pi f_0 t})}{8} \right) \\ &= h_3 \left(\frac{1}{4} \cos 6\pi f_0 t + \frac{3}{4} \cos 2\pi f_0 t \right) \end{aligned} \quad (43)$$

The resulting output of the parallel Hammerstein model $y[t]$, where the static constants h_i is replaced by filters $H_i[\omega]$, reads

$$y[t] = A_0 + A_1 \cos(2\pi f_0 t) + A_2 \cos(2 \cdot 2\pi f_0 t) + \dots + A_L \cos(L \cdot 2\pi f_0 t), \quad (44)$$

where the amplitudes A_q are given by

$$A_q = \begin{cases} \sum_{i=q}^L \left(\frac{1 + (-1)^q}{2} \right) \frac{1}{2^{i-1}} \left(\frac{i}{2} \right) H_i[qf_0] & q \text{ even} \\ \sum_{i=q}^L \left(\frac{1 - (-1)^q}{2} \right) \frac{1}{2^{i-1}} \left(\frac{i}{2} \right) H_i[qf_0] & q \text{ odd} \end{cases}. \quad (45)$$

For a pure sinusoid input signal, the amplitude A_1 is the fundamental tone and all A_q , where, $q \neq 1$ are distortion products. Thus, the figure of merit THD (and eventually $SFDR$) can be expressed as a function of the amplitudes, $THD=f(A_q)$

From the results in [Paper IV], the THD from the low code frequency component is

$${}^{LCF}THD = 20 \log_{10} \left(\frac{\sqrt{\sum_L |A_L|^2}}{A_1} \right). \quad (46)$$

The $SFDR$ is normally limited by the second or third harmonic given by (45).

The $SINAD$ is the ratio of the signal to the total noise. Unless otherwise specified, it is assumed to be the ratio of RMS signal to RMS noise, including harmonic distortion, for sine wave input signals. To study the effects of LCF , $SINAD$ is evaluated from the frequency domain.

Both the signal and the total noise can be determined from the discrete Fourier transform (DFT) of data records. Let $E[\omega]$ equal the residual spectrum of $Y[\omega]$ after the bins at $\omega_m=0$ (DC) and test frequencies, ω_i and $(\omega_s-\omega_i)$, have all been set to zero (excised from the spectrum). Then the RMS noise is found from the sum of all the remaining Fourier components,

$$rms \ noise = \frac{1}{N} \left[\sum_{m=0}^{N-1} |E[\omega_m]|^2 \right]^{\frac{1}{2}}. \quad (47)$$

The contribution to the noise from LCF is ${}^{LCF}THE$. The noise will thus be reduced to

$$rms \ noise = \frac{1}{N} \left[\sum_{m=0}^{N-1} \left(|E[\omega_m]|^2 - \sum_L |A_L|^2 \right) \right]^{\frac{1}{2}}. \quad (48)$$

The effects of the high code frequency component on THD and $SFDR$ can be evaluated in the frequency domain, these components can be described by a transfer function with an amplitude dependent piecewise constant amplification. How this will affect the harmonic distortion can be found from its DFT.

The effects of the high-code frequency component on $SINAD$ is evaluate based on the results from [47], where the maximum achievable $SINAD$ for a B -bit ADC is for a floating-point post correction given by (49)

$$SINAD = \frac{2^{2B}}{1 + 3 \cdot DNL_{RMS}^2}. \quad (49)$$

where DNL_{RMS} was developed in (6)

In [48], (49) was further developed to include a correction algorithm with a fixed-point resolution for correction values.

Assume that the errors due to the low code frequency component have been eliminated. That will give us from (40) the remaining $INL[k]$ to be ${}^{HCF}INL'[k]$

$${}^{HCF}INL'[k] = {}^{HCF}INL[k] + e[k]. \quad (50)$$

The differential nonlinearity $DNL[k]$ is found in equation (7), and since $\{e[k]\}$ are random variables independent and identically distributed, DNL_{RMS} yields

$$DNL_{RMS} = \frac{1}{2^{B-1}} \sum_{k=1}^{2^B-2} DNL^2[k] = \frac{1}{2^{B-1}} \sum_{k=1}^{2^B-2} {}^{HCF}DNL^2[k] + {}^{Error}DNL^2[k] \quad (51)$$

where ${}^{HCF}DNL[k]$ and ${}^{Error}DNL[k]$ is the $DNL[k]$ related to ${}^{HCF}INL[k]$ and $e[k]$, respectively. The potential for improvement from HCF is thus,

$${}^{HCF}DNL_{RMS} = \frac{1}{2^N - 2} \sum_{p=1}^P \left[\begin{array}{l} \{ \alpha_1[p]^2 (k_p - k_{p-1}) \} + \\ \left[\alpha_0[p] - \alpha_0[p-1] - \right. \\ \left. \alpha_1[p-1](k_{p-1} - 1 - k_{p-2}) \right] \end{array} \right]^2. \quad (52)$$

The improvement in terms of $SINAD$ is given by inserting (52) into (49).

The third component in (40) is considered as a zero mean, independent, identically distributed noise. Thus no harmonic distortion can be expected; only non harmonic distortion is present. The effect on THD will be zero, and this component affects $SINAD$ only. The potential for $SINAD$ improvement is [47]

$$SINAD = \frac{2^{2N}}{1 + 3 \cdot {}^{Error}DNL_{RMS}^2}. \quad (53)$$

and the RMS value of DNL was introduced in (6).

5 Discussion

Modeling analog to digital converters at radio frequency is the overall topic of this thesis, where the models are nonlinear dynamic behavior models aimed for post-correction. The content of this thesis includes the entire chain from design of test-bed and test scenarios, selection of model structure, characterization, a closed form solution of the parameter estimation problem, and an evaluation on the models usability for post-correction. Hence, the test-bed, method, and models are designed for the intended application area, namely radio frequencies.

The comprehensive picture is one contribution of this thesis. The comparison between different stimuli in Chapter 2 points out that multiple single tones is preferable as stimulus, even though it require several characterizations on different frequencies. In parallel with the stimuli evaluation, a suitable model structure was sought after. The model structure, which was developed by an independent test method (see Chapter 3), turned out to be easily characterized in a closed form with the preferred stimulus. Accordingly, results that at first sight are separate, act together in a coherent method for modeling ADC at radio frequency.

More specific contributions are the Cramér-Rao lower bound and the minimum variance estimator for histogram tests with an arbitrary stimulus. These results are universal and can be used in any application, with any stimulus. An interesting result is the introduction of the Kautz-Volterra model. The model has been successfully used for modeling power amplifiers and for pre-distortion, but have to my knowledge, previously not been used for ADCs. As future work, it will be interesting to apply the Kautz-Volterra model in a post-correction algorithm.

In the moment this thesis is written, some future work has already started. The closed form solution to the estimation problem will be improved [XV], and the dynamic integral nonlinearity model might be refined. The piecewise linear component is considered to be static throughout this thesis, partly motivated due to the use of a look-up table for post-correction. But since it is piece-wise linear, a parametric model-based post-correction may be used. Thus, a dynamic model might be taken under consideration that might improve the performance with only a few extra model parameters.

Summary of Appended Papers

The author has contributed in all aspects to the listed papers. In Paper VI, the first author has done a majority of the work although the thesis author has taken a significant part in the approach to the problem, simulations and writing process. Paper III and Paper VII are joint works.

PAPER I Truncated Gaussian noise in ADC histogram tests

One method to characterize analogue to digital converters (ADCs) is to use a histogram, in which Gaussian noise may be used as a stimulus signal. However, a Gaussian noise signal that excites all transition levels also generates input values outside working range of the ADC. Modern signal generators can generate arbitrary signals. Hence, excluding undesired values outside the ADC full scale can minimize test sequences. Truncating the signal to the working range gives further advantages, which are explored in this paper. The Cramér-Rao lower bound and a minimum variance estimator for histogram tests with an arbitrary stimulus are derived. These are applied for truncated Gaussian noise and the result is theoretically evaluated and compared to untruncated noise. It is shown that accuracy increases for a fixed sample length and that variation over transition levels decrease.

PAPER II Histogram Tests for Wideband Applications

Characterization and testing of analog-to-digital converters (ADCs) are important in many different aspects. The histogram test is a common method to characterize the linearity features of an ADC. Two commonly used stimuli signals are sine waves and Gaussian noise. This paper presents a metrological comparison between Gaussian and sine wave histogram tests for wideband applications; that is we evaluate the performance in characterization of the ADC and the usability of post-correction. A post-correction procedure involves characterization of the ADC non-linearity and then use of this information by processing the ADC output samples to remove the distortion.

The results show that the Gaussian histogram test gives reasonable accuracy to measure non-linearities. However, it does not result in a suitable model for post-correction in wideband applications. A single-tone sine wave histogram would be a better basis for post-correction. The best result can be obtained if the look-up table is trained with several single-tone sine waves in the frequency band.

PAPER III Measuring Volterra kernels of analog to digital converters using a stepped three-tone scan

Volterra theory can be used to mathematically model nonlinear dynamic components such as analog-to-digital converter (ADC). This paper describes how frequency domain Volterra kernels of an ADC are determined from measurements. The elements of Volterra theory are given and practical issues are considered, such as methods for signal conditioning, finding the appropriate test signals scenario and suitable sampling frequency. The results show that for the used pipeline ADC, the frequency dependence is significantly stronger for second order difference products than for sum products and the linear frequency dependence was not as pronounced as that of the second order Volterra kernel. It is suggested that the Volterra kernels have the symmetry properties of a specific box model, namely a parallel Hammerstein systems.

PAPER IV Achievable ADC performance by post-correction utilizing dynamic modeling of the integral nonlinearity

There is a need for a universal dynamic model of analog to digital converters (ADC) aimed for post-correction. However, it is complicated to fully describe the properties of an ADC in one model. An alternative is to split up the ADC model in different components, where each component has unique properties. In this paper, a model based on three components is used, and a performance analyze for each component is presented. Each component can be post-corrected individually and by the method that best suits the application. The purpose with post-correction of an ADC is to improve the performance. Hence, for each component, expressions for the potential improvement have been developed. The measures of performance are total harmonic distortion (*THD*) and signal to noise and distortion (*SINAD*). The results point out a gradual improvement as the components are successively corrected.

PAPER V High dynamic range test-bed for characterization of analogue-to-digital converters up to 500MSPS

A measurement set-up of for the characterization of analog-to-digital converters (ADCs) is described. The measurement set-up characterizes ADCs up to 16 bits at 350 MHz (option for >500 MHz). Testing dynamic performance of high-speed ADCs is regarded as difficult and expensive. By using existing state-of-the-art instruments in combination with specially designed amplifiers and filters, a high performance, cost efficient test-bed has been built-up. Practical performance corresponds to ADC datasheet and exceeds the performance obtained if using commercial instruments only. Consequently, the measurement results represent the true performance of the ADC without impact from the test-bed.

PAPER VI Model Based Dynamic Characterization Of Analog-Digital-Converters At Radio Frequency — Invited paper

A dynamic characterization of analog-digital converter integral nonlinearity (*INL*) is considered. When using a plurality of test frequencies in the measurement set-up, the dynamic errors of the converter are characterized. The *INL* is modeled by low and high code components – *LCF* and *HCF*, respectively. The *LCF* and *HCF* are parameterized and a least squares method is derived for the estimation of the parameter values from obtained measurements. A closed form solution to the estimation problem is derived and its performance is illustrated by a numerical example. The proposed method is believed to be fruitful in wide-band characterization of analog-digital converters at radio frequency, and thus of importance for the evaluation of modern and future wireless communication systems.

PAPER VII Kautz-Volterra modelling of an analogue-to-digital converter using a stepped three tone excitation

In many test and measurement applications, the analogue-to-digital converter (ADC) is the limiting component. Using post-correction methods can improve the performance of the component as well as the over all measurement system. In this paper an ADC is characterised by a Kautz-Volterra (KV) model, which utilises a model-based post-correction of the ADC with general properties and a reasonable number of parameters. Results that are based on measurements on a high-speed 12-bit ADC, shows good results for a third order model.

References

- [1] D. A. Rauth and V. T. Randal, "Analog-to-digital conversion. part 5," *IEEE Instrumentation & Measurement Magazine*, vol. 8, pp. 44-54, 2005.
- [2] E. Balestrieri, P. Daponte, and S. Rapuano, "A state of the art on ADC error compensation methods," in *IEEE Instrumentation And Measurement Technology Conference*, Como, Italy, 2004, pp. 711-716.
- [3] H. Lundin, M. Skoglund, and P. Händel, "A Criterion for Optimizing Bit-Reduced Post-Correction of AD Converters," *IEEE Transactions on Instrumentation and Measurements*, vol. 53, pp. 1159-1166, 2004.
- [4] H. Lundin, T. Andersson, M. Skoglund, and P. Händel, "Analog-to-digital converter error correction using frequency selective tables," in *RadioVetenskap och Kommunikation (RVK)*, Stockholm, Sweden, 2002, pp. 487-490.
- [5] F. H. Irons, D. M. Hummels, and S. P. Kennedy, "Improved compensation for analog-to-digital converters," *IEEE Transactions on Circuits and Systems*, vol. 38, pp. 958-61, 1991.
- [6] J. Tsimbinos and K. V. Lever, "Improved error-table compensation of A/D converters," *IEE Proceedings-Circuits, Devices and Systems*, vol. 144, pp. 343-9, 1997.
- [7] D. Moulin, "Real-time equalization of A/D converter nonlinearities," Portland, OR, USA, 1989, pp. 262-7.
- [8] IEEE, "Std 1241-2000 IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," 2000.
- [9] S. Rapuano, P. Daponte, E. Balestrieri, L. De Vito, S. J. Tilden, S. Max, and J. Blair, "ADC parameters and characteristics," *IEEE Instrumentation & Measurement Magazine*, vol. 8, pp. 44-54, 2005.
- [10] T. E. Linnenbrink, J. Blair, S. Rapuano, P. Daponte, E. Balestrieri, L. De Vito, S. Max, and S. J. Jilden, "ADC testing," *IEEE Instrumentation & Measurement Magazine*, vol. 9, pp. 39-49, 2006.
- [11] IEEE, "Std 1057-1994 IEEE Standard for Digitizing Waveform Recorders," 1994.
- [12] TelASIC, "TC1410, 14-bit, 240 MSPS Analog-to-Digital Converter," TelASIC Communications, 2004.
- [13] R. C. Martins and A. M. Cruz Serra, "The use of a noise stimulus in ADC characterization," in *IEEE Int. Conf. on Electronics, Circuits and Systems*, 1998, pp. 457-460.
- [14] M. d. G. C. Flores, M. Negreiros, L. Carro, and A. A. Susin, "INL and DNL Estimation based on Noise for ADC Test," *IEEE trans. on Instrumentation and Measurement*, vol. 53, pp. 1391-1395, october 2004.
- [15] S. M. Kay, *Fundamentals of Statistical Signal Processing: Estimation Theory*. Upper Sadle River, NJ: Prentice Hall, 1993.

- [16] J. Blair, "Histogram Measurement of ADC Nonlinearities Using Sine Waves," *IEEE trans. on Instrumentation and Measurement*, vol. 43, pp. 373-383, 1994.
- [17] R. Holcer, L. Michaeli, and J. Saliga, "DNL ADC Testing by the Exponential Shaded Voltage," *IEEE trans. on Instrumentation and Measurement*, vol. 52, pp. 946-949, June 2003.
- [18] J. Saliga, L. Michaeli, and R. Holcer, "Noise Influence on exponential Histogram ADC test," in *Workshop on ADC modelling and testing*, Athens, 2004.
- [19] D. Rönnow, D. Wisell, and M. Isaksson, "Three-Tone Characterization of Nonlinear Memory Effects in Radio Frequency Power Amplifiers," *IEEE trans. on Instrumentation and Measurement*, p. in press, 2007.
- [20] D. Rabijns, W. Van Moer, and G. Vandersteen, "Spectrally pure excitation signals: only a dream?," *IEEE Transactions on Instrumentation and Measurement*, vol. 53, pp. 1433-40, 2004.
- [21] D. Rabijns, G. Vandersteen, W. van Moer, Y. Rolain, and J. Schoukens, "Creating spectral pure signals for ADC-testing," in *IMTC 03*, 2003.
- [22] P. Carbone, E. Nunzi, and D. Petri, "Statistical Efficiency of the ADC Sinewave Histogram Test," *IEEE trans. on Instrumentation and Measurement*, vol. 51, pp. 849-852, 2002.
- [23] A. Moschitta, P. Carbone, and D. Petri, "Statistical Performance of Gaussian ADC Histogram Test," in *Int Workshop on ADC modelling and testing*, 2003, pp. 213-217.
- [24] P. Händel, M. Skoglund, and M. Pettersson, "A calibration scheme for imperfect quantizers," *IEEE Transactions on Instrumentation and Measurement*, vol. 49, pp. 1063-8, 2000/10/ 2000.
- [25] P. Arpaia, P. Daponte, and S. Rapuano, "A state of the art on ADC modelling," *Elsevier Computer Standards & Interfaces*, vol. 26, pp. 31-42, 2003.
- [26] J. Paduart, J. Schoukens, and L. Gomme, "On the Equivalence between some Block Oriented Nonlinear Models and Nonlinear Polynomial State Space Models," in *IEEE Instrumentation and Measurement Technology Warsaw*, 2007.
- [27] H. Lundin, M. Skoglund, and P. Händel, "Optimal index-bit allocation for dynamic post-correction of analog-to-digital converters," *IEEE Transactions on Signal Processing*, vol. 53, pp. 660-71, 2005.
- [28] J. S. Bendat, *Nonlinear systems techniques and applications*. New York: Wiley, 1998.
- [29] D. Mirri, G. Iuculano, F. Filicori, G. Pasini, and G. Vannini, "Modeling of non ideal dynamic characteristics in S/H-ADC devices," in *Proceedings of 1995 IEEE Instrumentation and Measurement Technology Conference - IMTC '95, 24-26 April 1995*, Waltham, MA, USA, 1995, pp. 27-32.
- [30] J. Tsimbinos, "Identification and compensation of nonlinear distortion," in *Institute of Telecommunications Research: University of South Australia*, 1995.
- [31] W. H. Kautz, "Network synthesis for specified transient response," M.I.T. Research Lab., Electronics, Cambridge, MA 1952.

- [32] R. Hacioglu and G. A. Williamson, "Reduced complexity Volterra models for nonlinear system identification," *EURASIP Journal on Applied Signal Processing*, vol. 2001, pp. 257-65, 2001.
- [33] M. Isaksson and D. Rönnow, "A Kautz-Volterra behavioral model for RF power amplifiers," San Francisco, CA, USA, 2006, p. 4 pp.
- [34] M. Isaksson and D. Rönnow, "A Parameter-Reduced Volterra Model for Dynamic RF Power Amplifier Modeling based on Orthonormal Basis Functions," *Int. J. RF and Microwave Computer-Aided Eng*, p. In press, 2007.
- [35] D. Rönnow and M. Isaksson, "Digital predistortion of radio frequency power amplifiers using Kautz-Volterra model," *Electronics Letters*, vol. 42, pp. 780-2, 2006.
- [36] S. Boyd, Y. S. Tang, and L. O. Chua, "Measuring Volterra kernels," *IEEE Transactions on Circuits and Systems*, vol. CAS-30, pp. 571-7, 1983/08/1983.
- [37] L. O. Chua and Y. Liao, "Measuring Volterra kernels. II," *International Journal of Circuit Theory and Applications*, vol. 17, pp. 151-90, 1989/04/1989.
- [38] J. Schoukens and T. Dobrowiecki, "Design of broadband excitation signals with a user imposed power spectrum and amplitude distribution," in *IMTC/98 Conference Proceedings. IEEE Instrumentation and Measurement Technology Conference*, St. Paul, MN, USA, 1998, pp. 1002-5.
- [39] M. Schetzen, *Volterra and Wiener Theories of Nonlinear Systems*. New York: John Wiley & Sons, 1980.
- [40] L. Michaeli, P. Michalko, and J. Saliga, "Unified ADC Nonlinearity Error Model for SAR ADC," *Measurement*, vol. In Press, Accepted Manuscript, p. Available online, 2006.
- [41] L. Michaeli, P. Michalko, and J. Saliga, "Identification of unified ADC error model by triangular testing signal," in *10th Workshop on ADC modelling and testing*, Gdynia/Jurata, Poland, 2005, pp. 605-610.
- [42] L. Michaeli, L. Sochová, and J. Saliga, "ADC look-up table based post correction combined with dithering," in *IMEKO World Congress Rio de Janeiro*, Brazil, 2006.
- [43] M. Isaksson, D. Wisell, and D. Rönnow, "Wide-band dynamic modeling of power amplifiers using radial-basis function neural networks," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, pp. 3422-8, 2005.
- [44] M. Isaksson, D. Wisell, and D. Rönnow, "A comparative analysis of behavioral models for RF power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, pp. 348-59, 2006.
- [45] P. Mikulik and J. Saliga, "Volterra filtering for integrating ADC error correction, based on an a priori error model," *IEEE Transactions on Instrumentation and Measurement*, vol. 51, pp. 870-5, 2002.
- [46] J. Tsimbinos and K. V. Lever, "Computational complexity of Volterra based nonlinear compensators," *Electronics Letters*, vol. 32, pp. 852-4, 1996.

- [47] N. Giaquinto, M. Savino, and A. Trotta, "Detection, digital correction and global effect of A/D converters nonlinearities," Smolenice Castle, Slovakia, 1996, pp. 122-7.
- [48] H. Lundin, P. Händel, and M. Skoglund, "Accurate Prediction of Analog-to-Digital Converter Performance After Post-Correction," in *IMEKO World Congress* Rio de Janeiro, Brazil, 2006.